Datasheet

G32R430

Cortex-M52 core beased 32-bit encoder-specific MCU

Version: Draft V0.3

1 Product Characteristics

Core

- Arm® Cortex®-M52 32-bit core
- Maximum operating frequency of 128MHz over the full temperature and voltage range
- Operating voltage: 1.7~3.6V
- Built-in 4KB Cache
- Built-in hardware TMU: Supports ATAN operation
- Support nested vector interrupt controller (NVIC)
- Support ITCM/DTCM extension

Memory and interface

- Flash: Up to 128KB
- TCM: Including 16KB DTCM and 32KB ITCM

Clock

- HSECLK: 8~26MHz external crystal/ceramic oscillator supported
- LSECLK: 32.768kHz crystal/ceramic oscillator supported
- HSICLK: 8MHz RC oscillator calibrated by factory
- LSICLK: 32kHz RC oscillator supported
- PLL: Phase Locked Loop Clock, with maximum output frequency 128MHz

Power supply and power supply management

- V_{DD} range: 1.7～3.6V
- V_{DDA} range: 1.7～3.6V
- Power-on/power-down reset (POR/PDR) supported
- Programmable voltage detector (PVD) supported
- Support main power detection (EVS)

Low-power mode

- Support stop and standby two low-power modes

DMA

- 1 DMA with 8 data streams

Debugging interface

- SWD

I/O

- Up to 48 I/O
- All I/O can be mapped to external interrupt vectors and awakened from STOP mode
- Up to 6 FT input I/O
- Up to 4 I/O support STANDBY wake-up

Communication peripherals

- 2 USART, with a maximum transmission rate of 16Msps, supporting automatic control of RS485 transmission enable
- 1 I2C, supporting up to 400kHz

- 1 SPI, with a maximum transmission rate of 50Mbit/s in master-slave mode

Analog peripherals

- 2 16-bit ADC, supporting regular sequence, injection sequence, single-shot and continuous sampling modes, master-slave mode, maintaining sampling synchronization when configuring master-slave, up to 6 pairs of differential/12 single-ended sampling channels
- 1 12-bit ADC, supporting up to 14 external channels and 2 internal channels
- 2 10-bit DAC, with DAC outputs configurable as comparator inputs
- 1 temperature sensor
- 4 programmable analog comparator (COMP)

Timer

- 1 16-bit advanced timer with up to 4 complementary channels, supporting input capture, output compare, braking, dead zone, PWM, and pulse counting
- 3 16-bit general-purpose timers, each with up to 4 independent channels to support input capture, output compare, PWM, pulse count and other functions
- 1 16-bit low-power timer
- 2 watchdog timers: One independent watchdog IWDT and one window watchdog WWDT

RTC

- Support calendar function
- Support alarm and regular wake-up from stop/standby mode

Chip package

- UFBGA64(5x5mm)
- QFN60(6x6mm)
- QFN48(7x7mm)
- QFN32(5x5mm)

Contents

2 Product Information

See the following table for product functions and peripheral configuration.

Table 1 Chip Functions and Peripherals

Product		**G32R430**			
Model		RBI7	UBU7	CBU7	KBU7
Package		UFBGA64	QFN60	QFN48	QFN32
Core and maximum working frequency		Arm® Cortex®-M52 32-bit @128MHz			
Working voltage		1.7~3.6V			
Memory (KB)		128			
DTCM (KB)		16			
ITCM (KB)		32			
TMU		1			
DMA		1			
GPIOs		48	45	34	21
Communication interface	USART	2			
	SPI	1			
	I2C	1			
Timer	16-bit advanced	1			
	16-bit general	3			
	16-bit low-power	1			
	24-bit counter (SysTick)	1			
	Watchdog	2 (IWDT+WWDT)			
Real-time clock (RTC)		1			
16-bit ADC	Unit	2			
	Channel	12	12	8	4
12-bit ADC	Unit	1			
	Channel	16	16	13	10
10-bit DAC	Unit	2			
	Channel	2			
Comparator		4			
Temperature sensor		1			
Operating temperature		Ambient temperature: -40℃ to 105℃ Junction temperature: -40℃ to 125℃			

3 Pin Information

3.1 Pin Distribution

Figure 1 Distribution Diagram of UFBGA64 Pins

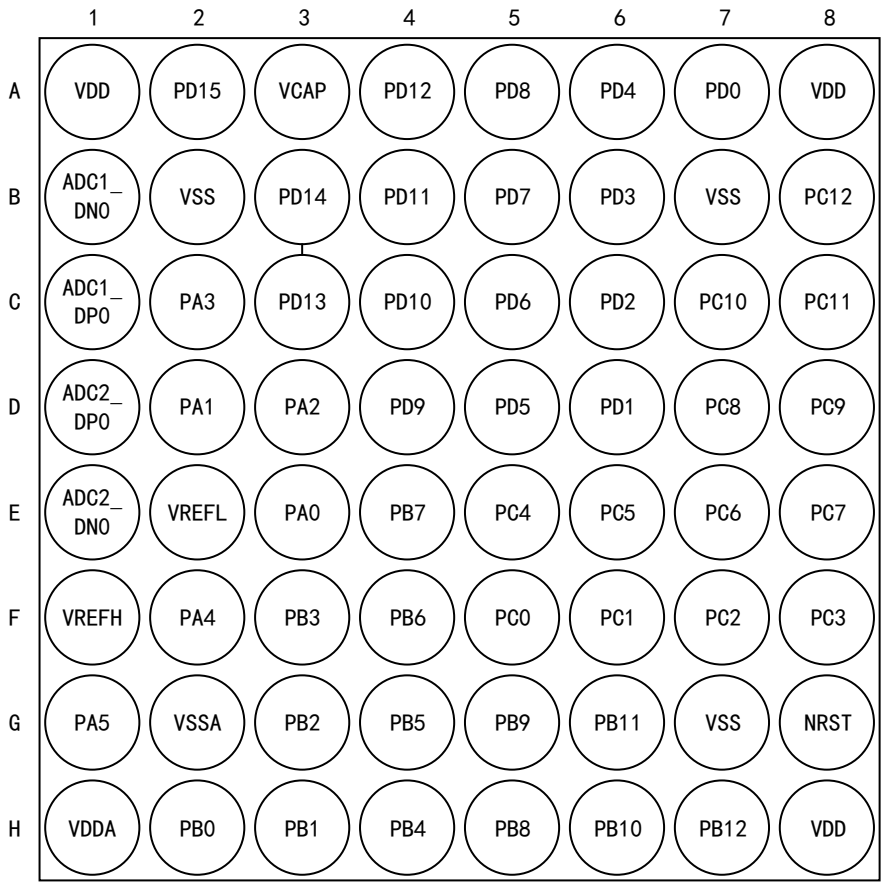


Figure 2 Distribution Diagram of QFN60 Pins

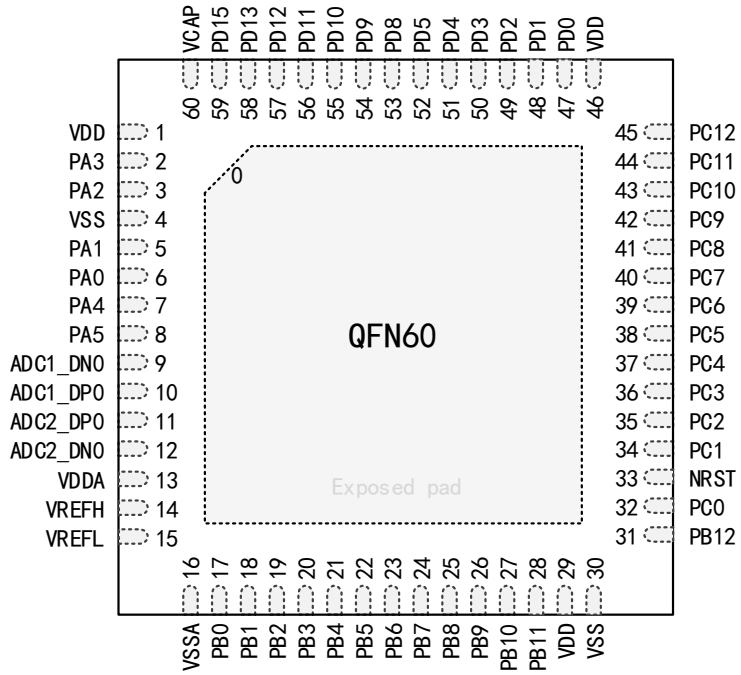


Figure 3 Distribution Diagram of QFN48 Pins

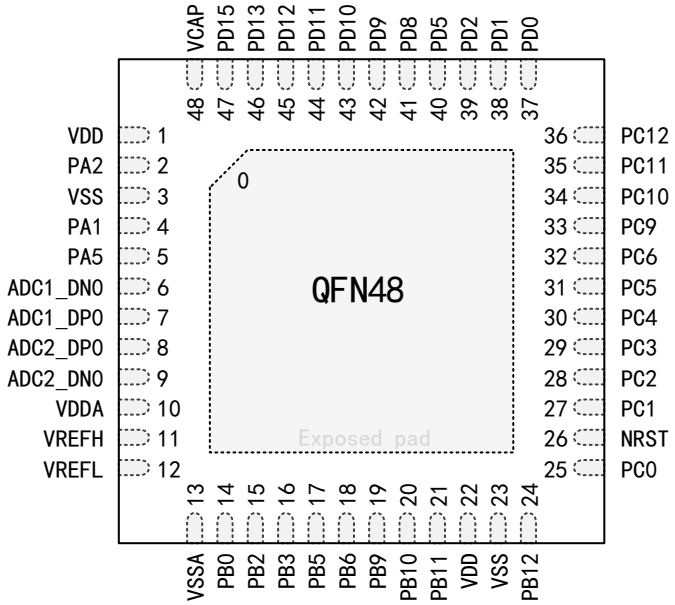
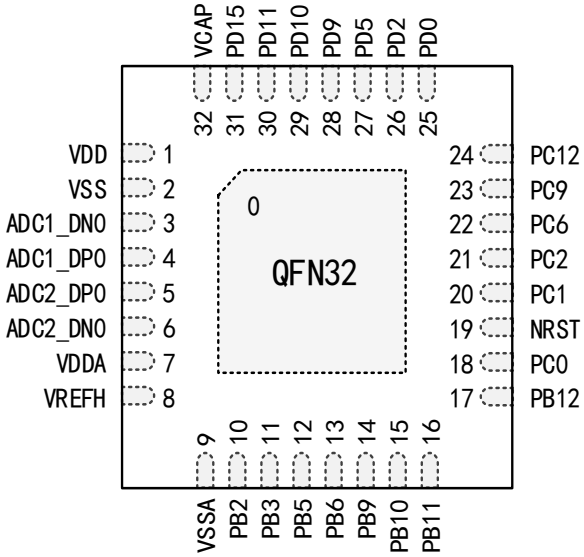


Figure 4 Distribution Diagram of QFN32 Pins



3.2 Pin Functional Description

Table 2 Legends/Abbreviations Used in Output Pin Table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in the bracket below the pin name, the pin functions during and after reset are the same as the actual pin name	
Pin type		P	Power supply pin
		I	Only input pin
		O	Only output pin
		I/O	I/O pin
I/O structure		5T	FT I/O
		STDA	3.3V standard I/O, directly connected to ADC
		STD	3.3V standard I/O
		B	Dedicated Boot0 pin
		RST	Bidirectional reset pin of built-in pull-up resistor
Caution		Unless otherwise specified in the notes, all I/O is set as floating input during and after reset	
Pin function	Default multiplexing function	Select/enable this function directly through peripheral register	
	Redefining function	Select this function through AFIO remapping register	

Table 3 Description in Pin Number Order

UFBGA64	QFN60	QFN48	QFN32	Pin name (Function after reset)	Type	Structure	Default function	Multiplexing function	Additional function
A1	1	1	1	VDD	P	-	VDD	-	-
C2	2	-	-	PA3	I/O	STD	ADC1_DN2	TMR2_CH4	ADC1_SE5
D3	3	2	-	PA2	I/O	STD	ADC1_DN1	TMR2_CH3	ADC1_SE4
B2	4	3	2	VSS	P	-	-	-	-
D2	5	4	-	PA1	I/O	STD	ADC1_DP1	TMR2_CH2	ADC1_SE1
E3	6	-	-	PA0	I/O	STD	ADC1_DP2	TMR2_CH1	ADC1_SE2
F2	7	-	-	PA4	I/O	STD	ADC2_DP2	TMR2_ETR	ADC2_SE2
G1	8	5	-	PA5	I/O	STD	ADC2_DP1	TMR2_CH4 TMR2_ETR	ADC2_SE1
B1	9	6	3	ADC1_DN0	I	-	ADC1_DN0	-	ADC1_SE3
C1	10	7	4	ADC1_DP0	I	-	ADC1_DP0	-	ADC1_SE0
D1	11	8	5	ADC2_DP0	I	-	ADC2_DP0	-	ADC2_SE0
E1	12	9	6	ADC2_DN0	I	-	ADC2_DN0	-	ADC2_SE3
H1	13	10	7	VDDA	P	-	VDDA	-	-
F1	14	11	8	VREFH	P	-	VREFH	-	-
E2	15	12	-	VREFL	P	-	VREFL	-	-
G2	16	13	9	VSSA	P	-	VSSA	-	-
H2	17	14	-	PB0	I	-	ADC2_DN1	-	ADC2_SE4
H3	18	-	-	PB1	I	-	ADC2_DN2	-	ADC2_SE5
G3	19	15	10	PB2	I/O	STD	PB2	USART1_CK TMR3_ETR TMR3_CH1	ADC3_CH0 COMP3_IP0 COMP3_IN0
F3	20	16	11	PB3	I/O	STD	PB3	I2C_SCL USART1_TX TMR3_CH1	ADC3_CH1 COMP3_IP1 COMP3_IN1
H4	21	-	-	PB4	I/O	5T	PB4	I2C_SDA USART1_RX TMR3_CH2	DAC1_OUT
G4	22	17	12	PB5	I/O	STD	SWCLK	I2C_SDA USART1_CTS TMR3_CH3	ADC3_CH2
F4	23	18	13	PB6	I/O	5T	PB6	USART1_RX TMR3_CH4 COMP1_OUT	COMP4_IN0
E4	24	-	-	PB7	I/O	STD	PB7	USART1_DE TMR2_CH1 TMR3_ETR	COMP4_IP0

UFBGA64	QFN60	QFN48	QFN32	Pin name (Function after reset)	Type	Structure	Default function	Multiplexing function	Additional function
H5	25	-	-	PB8	I/O	STD	PB8	TMR2_CH4	COMP4_IN1
G5	26	19	14	PB9	I/O	STD	PB9	USART1_TX TMR2_CH2 COMP2_OUT	COMP4_IP1
H6	27	20	15	PB10	I/O	STD	SWDIO	USART1_RTS TMR2_CH3 TMR1_CH1	-
G6	28	21	16	PB11	I/O	STD	PB11/NMI	USART1_DE USART1_CTS TMR1_CH2	-
H8	29	22	-	VDD	P	-	VDD	-	-
G7	30	23	-	VSS	P	-	VSS	-	-
H7	31	24	17	PB12	I/O	STD	HSE_IN	TMR3_ETR	-
F5	32	25	18	PC0	I/O	STD	HSE_OUT	TMR3_CH1	-
G8	33	26	19	NRST	I	RST	NRST	-	-
F6	34	27	20	PC1	I/O	STD	PC1/WUIO	I2C_SCL TMR3_CH2	LSE_IN
F7	35	28	21	PC2	I/O	STD	PC2/WUIO	I2C_SDA TMR3_CH3	LSE_OUT
F8	36	29	-	PC3	I/O	STD	PC3	TMR3_ETR SPI_CS	ADC3_CH0
E5	37	30	-	PC4	I/O	STD	PC4	TMR2_CH1 SPI_CS	ADC3_CH1
E6	38	31	-	PC5	I/O	STD	PC5	TMR4_ETR TMR2_ETR SPI_CLK	ADC3_CH2
E7	39	32	22	PC6	I/O	STD	PC6	USART2_TX TMR4_CH1 TMR3_CH1 SPI_CS	ADC3_CH3
E8	40	-	-	PC7	I/O	STD	PC7	TMR3_CH3	ADC3_CH4
D7	41	-	-	PC8	I/O	STD	PC8	TMR3_CH4	ADC3_CH5
D8	42	33	23	PC9	I/O	STD	PC9	USART2_CK TMR4_CH2 TMR3_CH2 SPI_CLK	ADC3_CH6
C7	43	34	-	PC10	I/O	STD	PC10	TMR4_CH3 TMR4_ETR SPI_MISO	ADC3_CH7

UFBGA64	QFN60	QFN48	QFN32	Pin name (Function after reset)	Type	Structure	Default function	Multiplexing function	Additional function
C8	44	35	-	PC11	I/O	STD	PC11	TMR4_CH4 SPI_MOSI	ADC3_CH8
B8	45	36	24	PC12	I/O	5T	PC12	USART2_RX TMR4_ETR CLK_OUT	ADC3_CH9
B7	-	-	-	VSS	P	-	VSS	-	-
A8	46	-	-	VDD	P	-	VDD	-	-
A7	47	37	25	PD0	I/O	STD	PD0/WUIO	USART2_TX TMR2_CH3	ADC3_CH10
D6	48	38	-	PD1	I/O	STD	PD1	USART2_TX TMR1_CH1	ADC3_CH11
C6	49	39	26	PD2	I/O	STD	PD2	I2C_SCL USART2_DE TMR1_CH1N SPI_MISO	ADC3_CH12
B6	50	-	-	PD3	I/O	STD	PD3	I2C_SDA TMR1_CH4	-
A6	51	-	-	PD4	I/O	STD	PD4	I2C_SMBA	ADC3_CH13
D5	52	40	27	PD5	I/O	5T	PD5	I2C_SCL USART2_RX TMR1_CH2 SPI_MOSI	DAC2_OUT
C5	-	-	-	PD6	I/O	STD	PD6	TMR1_CH2	-
B5	-	-	-	PD7	I/O	STD	PD7	USART2_CK TMR1_CH2N	-
A5	53	41	-	PD8	I/O	STD	PD8	I2C_SMBA USART2_DE TMR1_CH2N	-
D4	54	42	28	PD9	I/O	STD	PD9/WUIO	I2C_SDA USART2_TX TMR1_CH3	COMP2_IP1 COMP2_IN1
C4	55	43	29	PD10	I/O	STD	PD10	USART2_RTS USART1_DE TMR1_CH3N SPI_CS	COMP2_IP0 COMP2_IN0
B4	56	44	30	PD11	I/O	STD	PD11	USART2_CTS TMR1_ETR TMR1_BKIN SPI_CLK	COMP1_IP1 COMP1_IN1

UFBGA64	QFN60	QFN48	QFN32	Pin name (Function after reset)	Type	Structure	Default function	Multiplexing function	Additional function
A4	57	45	-	PD12	I/O	5T	PD12	USART1_RX TMR2_ETR EVENT_OUT	COMP1_IP0 COMP1_IN0
C3	58	46	-	PD13	I/O	STD	PD13	TMR4_CH1 TMR2_CH1 TMR1_CH4	-
B3	-	-	-	PD14	I/O	STD	PD14	USART1_CK TMR4_CH2 TMR2_CH2	-
A2	59	47	31	PD15	I/O	5T	EVS_VDC	USART1_TX USART1_DE TMR4_CH3	-
A3	60	48	32	VCAP	P	-	VCAP	-	-

Note:

(1) WUIO: Supports IO in standby mode

(2) EVS_VDC: External 5V DC Voltage Supervisor, used to supervise 5V power-on and power-down

3.3 GPIO Multiplexing Function Configuration

Table 4 Port A Multiplexing Function Configuration

Pin name	AF0	AF1	AF2	AF3
PA0	TMR2_CH1	-	-	-
PA1	TMR2_CH2	-	-	-
PA2	TMR2_CH3	-	-	-
PA3	TMR2_CH4	-	-	-
PA4	TMR2_ETR	-	-	-
PA5	TMR2_CH4	TMR2_ETR	-	-

Table 5 Port B Multiplexing Function Configuration

Pin name	AF0	AF1	AF2	AF3
PB0	-	-	-	-
PB1	-	-	-	-
PB2	USART1_CK	TMR3_ETR	TMR3_CH1	-
PB3	I2C_SCL	USART1_TX	TMR3_CH1	-
PB4	I2C_SDA	USART1_RX	TMR3_CH2	-
PB5	SWCLK	I2C_SDA	USART1_CTS	TMR3_CH3

Pin name	AF0	AF1	AF2	AF3
PB6	USART1_RX	TMR3_CH4	-	COMP1_OUT
PB7	USART1_DE	TMR2_CH1	TMR3_ETR	-
PB8	TMR2_CH4	-	-	-
PB9	USART1_TX	TMR2_CH2	-	COMP2_OUT
PB10	SWDIO	USART1_RTS	TMR2_CH3	TMR1_CH1
PB11	NMI	USART1_DE	USART1_CTS	TMR1_CH2
PB12	TMR3_ETR	-	-	-

Table 6 Port C Multiplexing Function Configuration

Pin name	AF0	AF1	AF2	AF3
PC0	TMR3_CH1	-	-	-
PC1	I2C_SCL	TMR3_CH2	-	-
PC2	I2C_SDA	TMR3_CH3	-	-
PC3	TMR3_ETR	SPI_CS	-	-
PC4	TMR2_CH1	SPI_CS	-	-
PC5	TMR4_ETR	TMR2_ETR	SPI_CLK	-
PC6	TMR4_CH1	TMR3_CH1	SPI_CS	USART2_TX
PC7	TMR3_CH3	-	-	-
PC8	TMR3_CH4	-	-	-
PC9	USART2_CK	TMR4_CH2	TMR3_CH2	SPI_CLK
PC10	TMR4_CH3	TMR4_ETR	SPI_MISO	-
PC11	TMR4_CH4	SPI_MOSI	-	-
PC12	USART2_RX	TMR4_ETR	CLK_OUT	-

Table 7 Port D Multiplexing Function Configuration

Pin name	AF0	AF1	AF2	AF3
PD0	USART2_TX	TMR2_CH3	-	-
PD1	USART2_TX	TMR1_CH1	-	-
PD2	I2C_SCL	USART2_DE	TMR1_CH1N	SPI_MISO
PD3	I2C_SDA	TMR1_CH4	-	-
PD4	I2C_SMBA	-	-	-
PD5	I2C_SCL	USART2_RX	TMR1_CH2	SPI_MOSI
PD6	TMR1_CH2	-	-	-
PD7	USART2_CK	TMR1_CH2N	-	-

Pin name	AF0	AF1	AF2	AF3
PD8	I2C_SMBA	USART2_DE	TMR1_CH2N	-
PD9	I2C_SDA	USART2_TX	TMR1_CH3	-
PD10	USART2_RTS	USART1_DE	TMR1_CH3N	SPI_CS
PD11	USART2_CTS	TMR1_ETR	TMR1_BKIN	SPI_CLK
PD12	USART1_RX	TMR2_ETR	EVENT_OUT	-
PD13	TMR4_CH1	TMR2_CH1	TMR1_CH4	-
PD14	USART1_CK	TMR4_CH2	TMR2_CH2	-
PD15	USART1_TX	USART1_DE	TMR4_CH3	-

4 Functional description

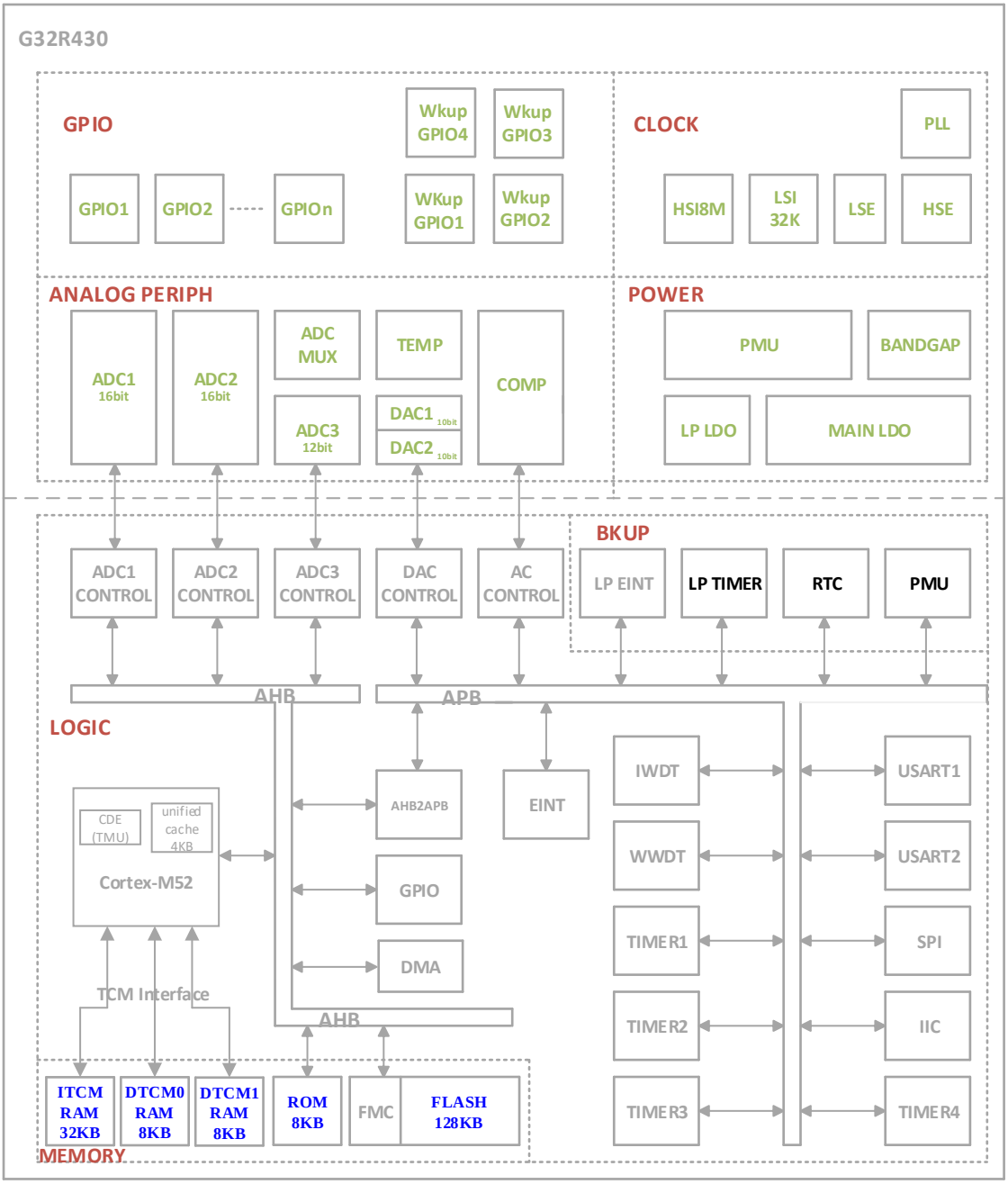
The G32R430 is a digital-analog hybrid MCU customized for high-precision magneto-electric/photoelectric absolute position encoders. Based on G32R430, high-precision magneto-electric/photoelectric absolute position encoders can be implemented. This chapter mainly introduces the G32R430 chip's system architecture, power supply, high-precision analog unit, real-time trigonometric acceleration unit, interrupts, on-chip memory, clocks, peripheral functions and characteristics.

The G32R430 is based on high-performance, low-power CPU Arm® Cortex®-M52, which uses Arm V8.1-M architecture. For information about the Arm® Cortex®-M52 core, please refer to the Arm® Cortex®-M52 technical reference manual, which can be downloaded from Arm's website.

4.1 System Architecture

4.1.1 System Block Diagram

Figure 5 System Block Diagram



4.1.2 Address Mapping

Table 8 Address Mapping

Area	Address range	Size	Peripheral name
AHB Bus	0x4002 1800 - 0x4002 1BFF	1KB	GPIO
	0x4002 1400 - 0x4002 17FF	1KB	ADC3（12bit）

Area	Address range	Size	Peripheral name
	0x4002 1000 - 0x4002 13FF	1KB	ADC2（16bit）
	0x4002 0C00 - 0x4002 0FFF	1KB	ADC1（16bit）
	0x4002 0800 - 0x4002 0BFF	1KB	FLASH Interface
	0x4002 0400 - 0x4002 07FF	1KB	RCM
	0x4002 0000 - 0x4002 03FF	1KB	DMA
APB Bus	0x4000 5800 - 0x4000 5BFF	1KB	DBGMCU
	0x4000 3C00 - 0x4000 3FFF	1KB	TS
	0x4000 3B00 - 0x4000 3BFF	256Bytes	LPTMR
	0x4000 3A00 - 0x4000 3AFF	256Bytes	RTC
	0x4000 3830 - 0x4000 39FF	208Bytes	BKP
	0x4000 3800 - 0x4000 382F	48Bytes	PMU
	0x4000 3400 - 0x4000 37FF	1KB	COMP
	0x4000 3000 - 0x4000 33FF	1KB	DAC2
	0x4000 2C00 - 0x4000 2FFF	1KB	DAC1
	0x4000 2800 - 0x4000 2BFF	1KB	EINT
	0x4000 2400 - 0x4000 27FF	1KB	IWDT
	0x4000 2000 - 0x4000 23FF	1KB	WWDT
	0x4000 1C00 - 0x4000 1FFF	1KB	I2C
	0x4000 1800 - 0x4000 1BFF	1KB	USART2
	0x4000 1400 - 0x4000 17FF	1KB	USART1
	0x4000 1000 - 0x4000 13FF	1KB	SPI
	0x4000 0C00 - 0x4000 0FFF	1KB	TMR4
	0x4000 0800 - 0x4000 0BFF	1KB	TMR3
	0x4000 0400 - 0x4000 07FF	1KB	TMR2
	0x4000 0000 - 0x4000 03FF	1KB	TMR1
Code	0x2000 0000 - 0x2000 3FFF	16KB	DTCM
	0x0800 0000 - 0x0801 FFFF	128KB	FLASH
	0x1FFF 0000 - 0x1FFF 000F	16Bytes	Option Bytes
	0x0010 0000 - 0x0010 1FFF	8KB	System Memory
	0x0000 0000 - 0x0000 7FFF	32KB	ITCM

4.1.3 Boot Configuration

The G32R430 supports booting from different storage areas. Users can select the boot mode by configuring the BOOTADDR [15:0] bits of Option Bytes.

To start up from BootLoader, the user can use serial interface to reprogram the user Flash. In embedded BootLoader mode, users can choose to reprogram the Flash through any of the following serial interfaces:

- USART1 (default interface) (PB6/PB9)

- USART2 (PD5/PD9)

4.2 Core

Arm® Cortex®-M52 is based on Arm® Cortex®-M series (including Cortex-M55 and Cortex-M85), which adopts Arm V8.1-M architecture. The efficiency is elevated to a new level. It also represents a significant milestone in introducing ML function to MCU.

4.3 Arithmetic Accelerator

4.3.1 Triangular Mathematical Unit (TMU)

The built-in trigonometric mathematics unit (TMU) currently supports ATAN instructions for computing angles to meet the requirements of encoder applications.

Table 9 ATAN Instruction Description

Instruction set	Equivalent operation	Instruction cycle
ATANOP32 a32, s32, c32, i16	a32=atan((s32/c32), i16)	80

Note:

(1) a32: The computed Atan value, formatted as a 32-bit fixed-point number in Q(1,31), represents an angle range of [-Pi, Pi]

(2) s32: SIN value, a 32-bit signed integer

(3) c32: COS value, a 32-bit signed integer

(4) I16: Instruction configuration word, including the number of iteration cycles

(5) For the Q(1,31) format result output by ATANOP32, the value range of a32 is [-1, 1], representing the angle range [- Pi, Pi]. For the usage of ATANOP32, please refer to the TMU documents in the G32R430 SDK. For more information about ATAN2, please visit the ATAN2 routine description in the G32R430 SDK.

4.4 Interrupt Controller

4.5 Nested Vectored Interrupt Controller (NVIC)

With 1 Nested Vectored Interrupt Controller (NVIC) built in, it is tightly coupled to the core, and enables efficient andlow-latency handling of exceptions, interrupts, and power management control. NVIC can handle up to 38 maskable interrupt channels (excluding 16 interrupt lines in Arm® Cortex®-M52) and 16 priorities; directly pass the interrupt vector entry address to the core; and support interrupt nesting.

4.5.1 External Interrupt/Event Controller (EINT)

The external interrupt/event controller consists of 23 edge detectors, and each detector includes edge detection circuit and interrupt/event request generation circuit; each detector can be configured as rising edge trigger, falling edge trigger or both and can be masked independently. Up to 48 GPIO can be connected to the 16 external interrupt lines.

4.6 On-chip Memory

The on-chip memory includes the main storage area, TCM (ITCM and DTCM), Option bytes, system storage area (ROM), and backup domain registers. The system storage area has been programmed before leaving the factory and cannot be erased or written.

Table 10 On-chip Memory Area

Memory	Maximum capacity	Function
Main memory area	128KB	Store user programs and data
TCM	48KB	CPU can access (read/write) with 0 wait cycle, 16KB DTCM, 32KB ITCM
System memory area	8KB	Store BootLoader program
Option byte	4Bytes	Configure main memory area read-write protection and MCU working mode
Backup domain register	32Bytes	Can be used to store data in STANDBY mode

4.6.1 Flash

The main storage area of the G32R430 on-chip memory is a 128KB embedded flash block, which is 32-bit wide and has sector/chip erase and programming capabilities, and can be used to store programs and data. It supports single-page erase and mass erase. At a junction temperature of 125℃, the minimum write/erase cycle is 100,000 cycles, and data can be retained for more than 10 years.

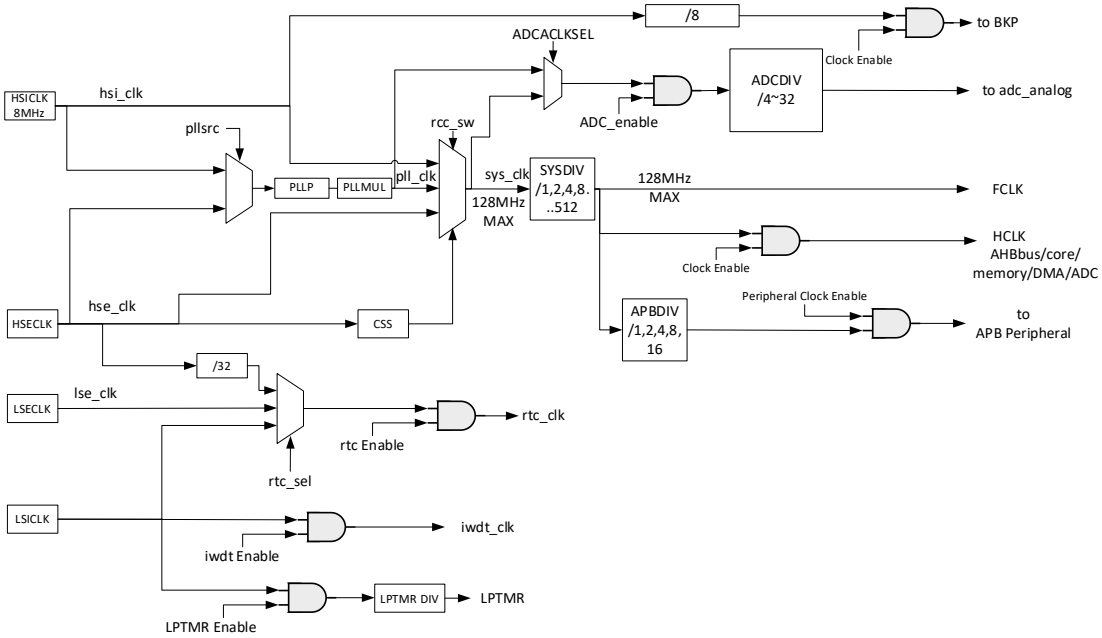
4.6.2 TCM

TCM is tightly coupled with the core, provides faster access speeds, and are typically used to store critical codes and data that require high-speed access or low latency. The G32R430 includes 16KB of DTCM and 32KB of ITCM, which can be accessed in byte, half word (16 bits), or full words (32 bits).

4.7 Reset and Clock

4.7.1 Clock Tree

Figure 6 Clock Tree



4.7.2 Clock Source

Clock sources are classified into high-speed clocks and low-speed clocks according to speed. High-speed clocks include HSICLK and HSECLK, while low-speed clocks include LSECLK and LSICLK.

4.7.3 System Clock

HSICLK, PLLCLK and HSECLK can be selected as system clock; the clock source of PLLCLK can be HSICLK or HSECLK; the requirred system clock can be obtained by configuring PLL clock multiplier factor and frequency division factor.

When the product is reset and started, HSICLK is selected as the system clock by default, and then the user can choose one of the above clock sources as the system clock by himself. When HSECLK failure is detected, the system will automatically switch back to HSICLK. If the interrupt is enabled, the software can receive the corresponding interrupt.

4.7.4 Bus Clock

AHB and APB buses are built in. The clock source of AHB is SYSCLK, and the clock source of APB is FCLK; the required clock can be obtained by configuring the frequency division factor. The maximum frequency of AHB is 128MHz, that of APB is 128MHz, and that of BKP domain is 1MHz. In addition, ADC requires a fixed frequency clock of around 20MHz. The required clock frequency can be obtained by enabling PLLCLK and configuring ADCDIV.

4.7.5 Phase-Locked Loop

The G32R430 series has 1 phase-locked loop (PLL). It requires configuration of parameters to generate different clock frequencies, with a maximum output frequency of 128 MHz. HSECLK or HSICLK can be used as the clock source for PLL.

4.7.6 Reset

There are three types of reset, defined as system reset, power reset, and backup domain reset.

For detailed information on reset, please refer to the Reset Management Unit (RMU) in the G32R430 User Manual.

4.8 Power Supply and Power Supply Management

4.8.1 Power Supply Scheme

Table 11 Power Supply Scheme

Name	Voltage range	Description
VDD	1.7～3.6V	Power the I/O (see the pin distribution diagram for specific IO) , LSICLKand internal voltage regulator through VDD pin.
V_{DDA}/V_{SSA}	1.7～3.6V	Supply power to the analog parts of ADC, DAC, LSECLK, RC oscillator, and PLL. When using a 16-bit ADC, V_{DDA} shall not be lower than 3.0V. When using EVS, the VDD should not be lower than 3.0V. When using HSECLK, TSE, ADC12B, COMP, or DAC, V_{DDA} shall not be lower than 2.7V.

4.8.2 1.2V Voltage Regulator

Table 12 Operating Mode of Voltage Regulator

Name	Description
Main mode (MR)	Used in run mode
Low-power mode (LPR)	Used in stop mode
Power-down mode	Used in standby mode; then the voltage regulator has high-impedance output, the core circuit is powered down, the power consumption of the voltage regulator is zero, and all data of registers and TCM will be lost.

Note:

(1) The voltage regulator is always in working state after reset, and outputs with high impedance in power-down mode.

(2) The equipment supports dynamic voltage scaling to optimize the power consumption in operating mode. The voltage of the main voltage regulator providing logic (VCORE) can be adjusted according to the maximum operating frequency of the system.

4.8.3 Power Supply Voltage Detector

The product integrates power-on reset (POR) and power-down reset (PDR) internally. These two circuits are always in working state. When the power-down reset circuit detects that the

power supply voltage is lower than the specified threshold value (V_{POR}/PDR), even for the external reset circuit, the system will remain reset.

The product includes a Programmable Voltage Detector (PVD) that can monitor V_{DD} and compare it with the PVD threshold. When V_{DD} is outside the PVD threshold range and the interrupt is enabled, an interrupt will be generated, and the MCU can be set to a safe state through the interrupt service program.

4.8.4 Main power Detection Module

The product integrates an External Voltage Supervisor (EVS) module. This module can detect the power-down and power-on of the main power when the external power supply of the entire system is input through the main power detection pin of the chip. The voltage for detecting the main power input can be configured into four different levels through registers. At the same time, when the main power is powered on or powered down, it can also trigger an interrupt.

4.9 Low-power Mode

The G32R430 supports stop and standby two low-power modes. These two modes have differences in power consumption, wake-up process, wake-up duration, and wake-up method. The low-power mode can be selected according to actual application needs.

The backup domain contains 16 16-bit registers, which can be used to store 32 bytes of data. In low-power mode, the stored information will not be lost, so it can be used to store important data.

4.10 DMA

1 DMA is built in, with a total of 8 channels. Each channel can be configured to connect different peripherals, but each channel can only enable one peripheral request at a time. Each channel can set priority, and the arbiter can coordinate the priority of corresponding DMA requests of each channel according to the priority of the channels. Data can be quickly transmitted through DMA without any CPU operation, and idle CPU resources can be reserved for other operations.

The peripherals that support DMA requests include: 16-bit ADC1/2, 12-bit ADC, SPI, USART1/2, I2C, and TMR1/2/3/4. Four levels of DMA channel priority can be configured. Data transmission of "Memory → Memory, Memory → Peripheral, Peripheral → Memory" is supported (memory includes Flash and SRAM).

4.11 GPIO

GPIO is a general-purpose input/output port that can control input and output via software. It supports configuration as general-purpose input, general-purpose output, multiplexing function, and analog input/output. Its general-purpose input can be configured as floating, pull-up, or pull-down input, and its general-purpose output can be configured as push-pull or open-drain output. GPIO can also be configured with pull-up/pull-down resistors and different rates (2MHz, 10MHz, and 50MHz). It has status latch and reset characteristics in STOP and STANDBY modes,

respectively. All GPIO can be used as external interrupts to wake up STOP mode. When the reset function is not enabled, the general-purpose I/O port is configured as the analog input mode. After reset, the debugging pin PB5 is put in the input pull-down mode, while PB10 is put in the pull-up mode.

4.12 Communication Peripherals

4.12.1 USART

2 universal synchronous/asynchronous transceivers are built in, supporting standard asynchronous communication and multiprocessor communication modes. They offer a wide range of baud rates and full duplex/half duplex data exchange capabilities, supporting NRZ standard format. Their serial port characteristics are configurable and have parity control and status detection functions. Speed and clock tolerance are achieved through programmable 8x or 16x oversampling rates, with independent transmit and receive enable. The baud rate is configured using a 16-bit division factor, and it also supports DMA continuous communication, multiprocessor wake-up, synchronous transmission, hardware flow control, and automatic I/O control of RS485 transmit enable.

4.12.2 I2C

One I2C bus interface is built in, providing multi-master function and controlling all I2C bus-specific sequencing, protocols, arbitration, and timing. It can operate in multi-master or slave mode, supports 7-bit or 10-bit addressing, and dual slave address addressing in 7-bit slave mode. The communication rate supports standard mode (up to 100kHz) and fast mode (up to 400kHz).

4.12.3 SPI

One SPI is built in, providing data transmission and reception functions based on the SPI protocol. It supports full-duplex and half-duplex communication in both master and slave modes, and can use the DMA controller. It can be configured with 8 or 16 bits per frame, and supports a maximum communication rate of 50Mbit/s. DMA operations can be used.

4.13 Analog Peripherals

4.13.1 16-bit ADC

The two ADC support master-slave synchronization mode, with sampling synchronized. The trigger methods include software or hardware triggers for dual ADC synchronous sampling. The external reference voltage input range is independent of the power supply. The ADC also supports various advanced general configurations, such as single or continuous/discontinuous scanning, multi-channel conversion, storage of results in TCM through DMA, adjustable sampling time, analog watchdog, and offset compensation.

4.13.2 12-bit ADC

One 12-bit ADC module is built in. It supports 16 single-ended sampling channels, and achieves a conversion rate of up to 1Msps. There are various triggering methods, including on-chip timers,

external pins, or software triggers. It supports the conversion between single and scan modes. It supports DMA requests for rule data conversion, and utilizes an analog watchdog to monitor the conversion voltages of multiple channels. The timer can be used to synchronize the analog-to-digital conversion with the clock.

4.13.3 Temperature sensor

A temperature sensor (Tsensor) with an independent module is built in and can be configured with different rates to generate data. Once the data is generated, an interrupt can be triggered.

4.13.4 LTCBG

A LTCBG module is built in and can output a stable voltage. The chip inside is directly connected to the channel ADC_CH15 of the 12-bit ADC.

4.13.5 DAC

Two 10-bit DAC modules are built in. Each DAC supports one output channel, and the DAC output can be connected to the comparator input. They support external signal triggering and internal timer triggering. Data can be left-aligned or right-aligned, and has synchronous update function. The dual DAC channels can convert independently or synchronously. The maximum external output rate is 200Ksps, while the internal output rate can reach up to 1Msps.

4.13.6 Comparator (COMP)

Four fast trail-to-rail comparators (COMP) are built in. All of them can be configured with parameters such as hysteresis, rate, and output polarity. The input voltage can be selected from external I/O or DAC output channels. The comparator outputs can be connected to I/O ports or to internal 16-bit timers for counting. Furthermore, the comparator outputs are internally connected to the extended interrupt and event controller. Each comparator has its own EINT signal line that can trigger interrupt events.

4.14 Timer

One 16-bit advanced timer, three 16-bit general-purpose timers, one independent watchdog timer, one window watchdog timer, one low-power timer, and one system tick timer are built in.

The advanced timer can be used to measure the pulse length of input signals (input capture), brake input, encoder interface, ETR input, or generate output waveforms (output compare, single-pulse output, complementary PWM with dead time insertion, or regular PWM output), or as a repeatable-counting time base.

The general-purpose timers can be used to measure the pulse length of input signals (input capture), encoder interface, ETR inputs, or generate output waveforms (output compare, single pulse output, ordinary PWM output), or as a simple time base.

The watchdog timer can be used to detect whether the program is running normally.

The low-power timer can operate and wake up the system in stop mode.

The system tick timer is the peripheral of the core with automatic reloading function. When the

counter is 0, it can generate a maskable system interrupt, which can be used for real-time operating system and general delay.

A comparison of the characteristics and functions among different timers is shown in the table below:

Table 13 Function Comparison of Timers

Timer type	Advanced timer	General-purpose timer	Low-power timer	System tick timer
Timer name	TMR1	TMR2/3/4	LPTMR	SysTick Timer
Clock source	Internal clock, external input, external trigger, internal trigger	Internal clock, external input, external trigger, internal trigger	Internal clock	Internal clock
Counter resolution	16 bits	16 bits	16 bits	24 bits
Counter type	Up, down, up/down	Up, down, up/down	Up	Down
Prescaler factor	Any integer between 1 and 65536	Any integer between 1 and 65536	Any integer between 1 and 65536	None
Internal trigger output	1	1	0	0
Generate DMA request	Can	Can	Cannot	Cannot
Capture/compare channel	4	4	0	0
Complementary output	3	None	None	None
Pin characteristics	1-way external trigger signal input pin; 1-way braking input pin; 3-group complementary channel pins; 1-way non-complementary channel pin.	1-way external trigger signal input pin; 4-way non-complementary channel pin.	None	None

Function Description	Each timer has 4 independent channels for input capture/output compare. The input capture supports counting function, PWM input, or encoder interface mode; the output compare supports PWM output, forced output, or single-pulse mode. It supports synchronization or event linking functions, enabling synchronous operation, and supports multiple slave modes and synchronization signals. It includes three complementary outputs with programmable dead time. One brake input is provided, which can also be configured as bidirectional mode. The repetition count function is available, and an update event can be generated after a configurable number of counting cycles. The counter can be frozen in debug mode. When an update event, trigger event, input capture/output compare event, or brake event occurs, an interrupt or DMA request can be generated. Each timer has an independent DMA request mechanism for generation. The comparator output can be connected to a timer for counting. It supports the positioning purpose of incremental (orthogonal) encoders and Hall sensor circuits.	Each timer has 4 independent channels for input capture/output compare. The input capture supports counting function, PWM input, or encoder interface mode; the output compare supports PWM output, forced output, or single-pulse mode. It supports synchronization or event linking functions, enabling synchronous operation, and supports multiple slave modes and synchronization signals. The counter can be frozen in debug mode. When an update event, trigger event, or input capture/output compare event occurs, an interrupt or DMA request can be generated. Each timer has an independent DMA request mechanism for generation. The comparator output can be connected to a timer for counting. It supports the positioning purpose of incremental (orthogonal) encoders and Hall sensor circuits. It supports ETR input, i.e. external trigger input function, which can be used as external clock or cycle-by-cycle current management.	It can operate in low-power mode and can be configured with a low-power timer interrupt to asynchronously wake up the system from the low-power mode. 16-bit time counting of prescaler can be configured.	It is specially used for real-time operating system. It has automatic reloading function. When the counter is 0, it can generate a maskable system interrupt. Clock source can be programmed.

Timer type	Advanced timer	General-purpose timer	Low-power timer	System tick timer
	It supports ETR input, i.e. external trigger input function, which can be used as external clock or cycle-by-cycle current management.			

Table 14 Function Comparison between IWDT and WWDT

Name	Counter resolution	Counter type	Prescaler factor	Functional description
Independent watchdog	12 bits	Down	Any integer between 1 and 256	The clock is provided by an internally independent RC oscillator of 32kHz, which is independent of the master clock, so it can run in stop mode. The whole system can be reset in case of any problems. It can provide timeout management for applications as a free-running timer. It can be configured as a software or hardware startup watchdog through option bytes. The counter can be frozen in debug mode.
Window watchdog	7 bits	Down	-	It can be set for free running. The whole system can be reset in case of any problems. Driven by the master clock, it has early warning interrupt function; The counter can be frozen in debug mode.

4.15 RTC

Real-time clock (RTC) is a timer that automatically switches to the backup power supply and maintains operation after the main power supply powers down. It has a set of continuously running counters, which can provide alarm interrupt and periodic interrupt functions together with software. RTC supports three types of clock sources. System reset or wake-up from standby mode will not cause RTC reset, ensuring its continuous and stable maintenance of time information.

4.16 Backup Register

The backup domain contains 16 16-bit registers, which can be used to store 32 bytes of data. The backup domain register is powered by a low-power LDO. System resetting, NRST pin resetting, and resetting after the low mode is waken up will not affect the backup domain register.

5 Electrical Characteristics

5.1 Test Conditions of Electrical Characteristics

5.1.1 Maximum and minimum values

Unless otherwise specified, all products are tested on the production line at T_A=25℃. Its maximum and minimum values can support the worst ambient temperature, power supply voltage and clock frequency.

The notes at the bottom of each table indicate that the data are obtained through comprehensive evaluation, design simulation or process characteristics and are not tested on the production line; on the basis of comprehensive evaluation, after passing the sample test, the average value is taken and three times the standard deviation (average $\pm 3\Sigma$) is added or subtracted to get the maximum and minimum values.

5.1.2 Typical value

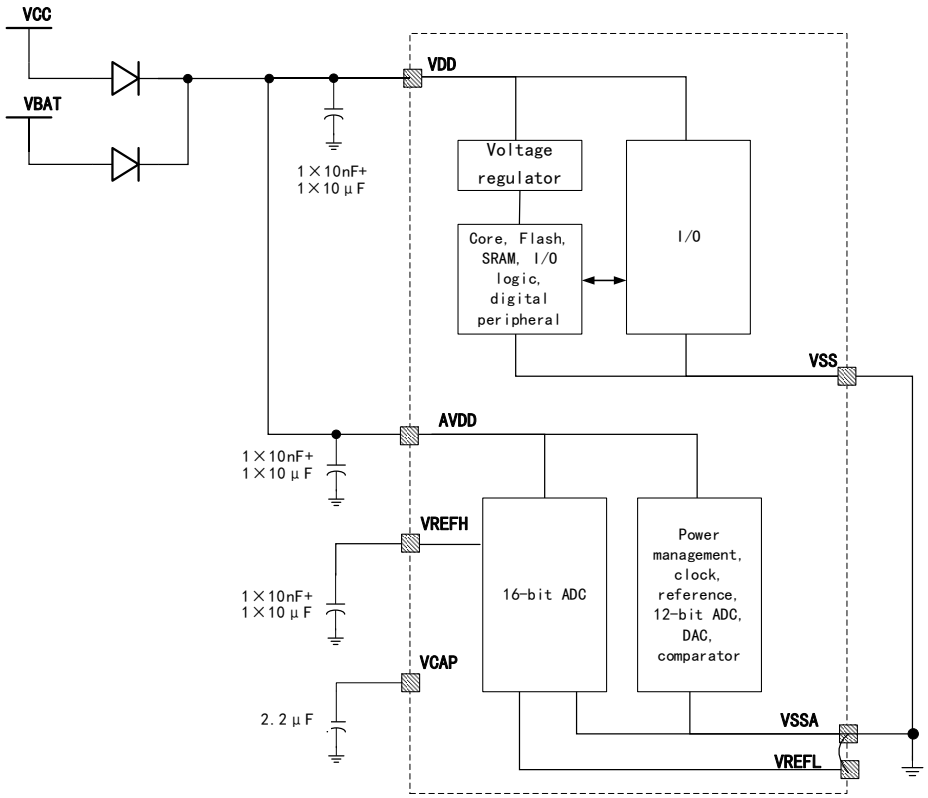
Unless otherwise specified, typical data are measured based on T_A=25℃, V_{DD}=V_{DDA}=3.3V. These data are only used for design guidance.

5.1.3 Typical curve

Unless otherwise specified, typical curves can only be used for design guidance and are not tested.

5.1.4 Power supply scheme

Figure 7 Power Supply Scheme



5.1.5 Load capacitance

Figure 8 Load Conditions When Measuring Pin Parameters

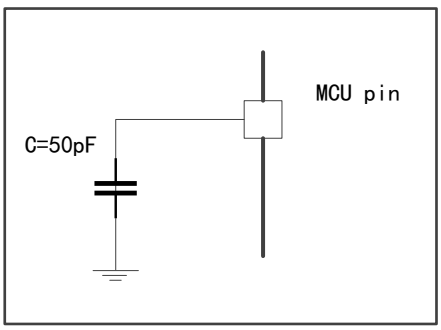


Figure 9 Pin Input Voltage Measurement Scheme

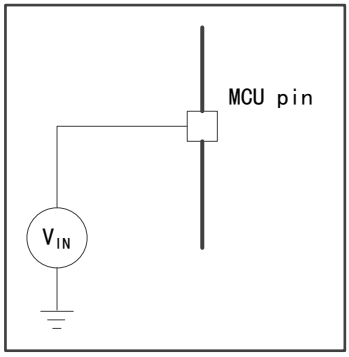
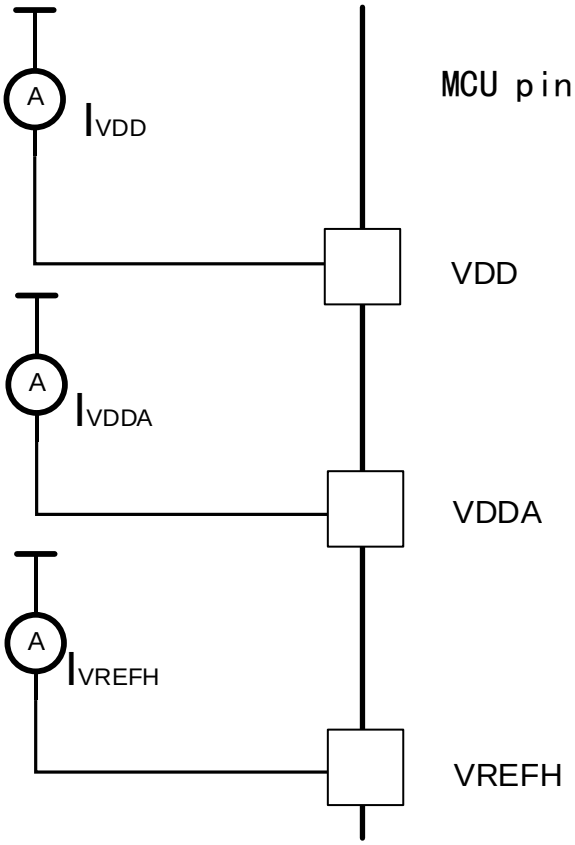


Figure 10 Power Consumption Measurement Scheme



5.2 Test under General Operating Conditions

Table 15 General Operating Conditions

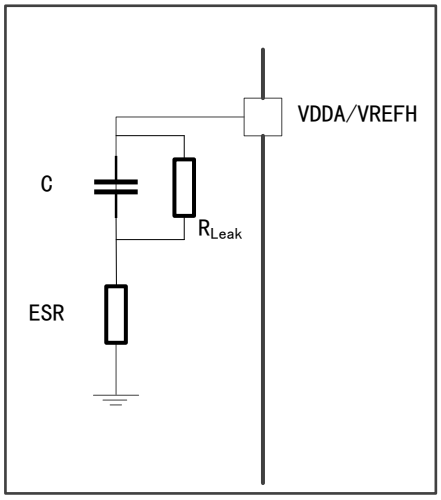
Symbol	Parameter	Condition	Min value	Typ value	Max value	Unit
f_{HCLK}	AHB clock frequency	-	-	-	128	MHz
f_{PCLK}	APB clock frequency	-	-	-	128	
f_{BKP}	BKP clock frequency	-	-	1	-	
V_{DD}	Main power supply voltage	-	1.7	-	3.6	V

Symbol	Parameter	Condition	Min value	Typ value	Max value	Unit
V_{DDA}	Analog power supply voltage (16-bit ADC not used)	-	1.7	-	3.6	V
	Analog power supply voltage (16-bit ADC working normally)		3.0	-	3.6	
T_A	Ambient temperature	Maximum power dissipation	-40	-	105	℃

5.3 External Capacitor

The stability of the ADC internal voltage reference source is achieved by connecting the external capacitor C_{EXT} to the VDDA_REFH pin. The typical value of C_{EXT} is 10uF, and the equivalent series resistance ESR of the capacitor is less than 1 Ω.

Figure 11 External Capacitor C_{EXT}



5.4 Absolute Maximum Rated Value

If the load on the device exceeds the absolute maximum rated value, permanent damage may be caused to the device. Here, only the maximum load that can be borne is given, and there is no guarantee that the device functions normally under this condition.

5.4.1 Maximum temperature characteristics

Table 16 Temperature Characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	-55 ~ +150	℃
T_J	Maximum junction temperature	125	

5.4.2 Maximum rated voltage characteristics

All power supply (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the

power supply within the external limited range.

Table 17 Maximum Rated Voltage Characteristics

Symbol	Description	Min value	Max value	Unit
V_{DD} - V_{SS}	External main power supply voltage	-0.3	4.0	V
V_{IN}	Input voltage on pins with 5V tolerance and 3.3V standard I/O	V_{SS}-0.3	5.5	
	Input voltage on other pins	V_{SS}-0.3	V_{DD}+0.3	
$\lvert \Delta V_{DDx} \rvert$	Voltage difference between different power supply pins	-	50	mV
$\lvert V_{SSx}-V_{SS} \rvert$	Voltage difference between different grounding pins	-	50	

5.4.3 Maximum rated current characteristics

Table 18 Current Characteristics

Symbol	Description	Max value	Unit
I_{VDD}	Sum of total current through V_{DD}/V_{DDA} power lines (1)	150	mA
I_{VSS}	Sum of total current through VSS ground line (1)	-150	
I_{IO}	Sink current on any I/O and control pin	25	
	Source current on any I/O and control pin	-25	
$I_{INJ(PIN)}$ (2)	Injection current of 3.3V standard I/O and 5T pin (3)	-5/+5	
	Injection current of NRST pin (3)		
$\Sigma I_{INJ(PIN)}$	Total injection current on all I/O and control pins (4)	±25	

Note:

(1) All power supplies (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SA}) must always be within the allowed range.

(2) The outflow current will interfere with the analog performance of the device.

(3) If V_{IN} exceeds the maximum value, $I_{INJ(PIN)}$ must be externally limited so that it does not exceed the maximum value. When V_{IN}>V_{DD}, the current flows into the pins; when V_{IN}<V_{SS}, the current flows out of the pins.

(4) When the current is injected into several I/O ports at the same time, the maximum value of $\Sigma I_{INJ(PIN)}$ is the sum of instantaneous absolute value of inflow current and outflow current.

5.4.4 Electrostatic discharge (ESD)

Table 19 ESD Absolute Maximum Ratings (1)

Symbol	Parameter	Condition	Range	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A=+25 ℃, conforming to ANSI/ESDA/JEDEC JS-001-2017	±4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging device model)	T_A=+25 ℃, conforming to ANSI/ESDA/JEDEC JS-002-2018	±1000	

Note: (1) The samples are measured by a third-party testing organization and are not tested in production.

5.4.5 Latch-up (LU)

Table 20 Latch-up (1)

Symbol	Parameter	Condition	Type
LU	Latch-up	T_A = 105℃, conforming to JEDEC JESD78F-2022	Class II A

Note: (1) The samples are measured by a third-party testing organization and are not tested in production.

5.5 On-chip Memory

5.5.1 Flash characteristics

Table 21 Flash Memory Characteristics (1)

Symbol	Parameter	Min value	Typ value	Max value	Unit
t_{prog}	32-bit programming time	-	84.7	-	μs
t_{ERASE}	Sector erase time	-	5.7	-	ms
t_{SBE}	Block erase time	-	8.2	-	
t_{SCE}	Mass erase time	8	-	10	
V_{prog}	Programming voltage	1.7	-	3.6	V
N_{END}	Number of erase cycles (Tj=125℃)	100	-	-	1,000 cycles
t_{RET}	Data retention period (Tj=125℃)	10	-	-	Year

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

5.6 Clock

5.6.1 Characteristics of external clock sources

5.6.1.1 High-speed external clock

8~26 MHz crystal/ceramic resonant oscillators can be used for high-speed external (HSECLK) clocks. In the applications, the resonator and load capacitor must be as close as possible to the oscillator pins to minimize output distortion and startup stabilization time.

Table 22 Characteristics of HSECLK 8~26MHz Oscillator (1)

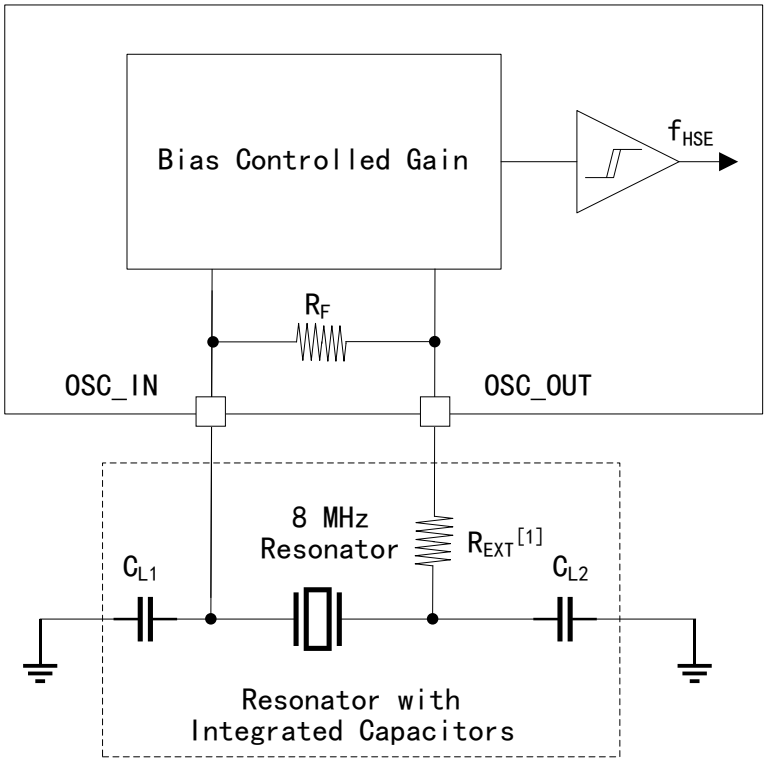
Symbol	Parameter	Condition	Min value	Typ value	Max value	Unit
f_{OSC_IN}	Oscillator frequency	-	8	-	26	MHz
R_F	Feedback resistance	-	-	200	-	kΩ
$I_{DD(HSECLK)}$	HSECLK current consumption	V_{DD}=3.3V, R_m=30Ω, C_L=10pF@8MHz	0.21	0.26	0.36	mA
Gm	Transconductance of oscillator	-	-	-	13	mA/V

Symbol	Parameter	Condition	Min value	Typ value	Max value	Unit
$t_{SU(HSECLK)}$	Startup time	V_{DD} is stable	-	1	5	ms

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

For CL1 and CL2, it is recommended to use high-quality external ceramic capacitors within the range of 5pF to 20pF (typical values), designed for high-frequency applications, and select according to the requirements of the crystal or resonator. CL1 and CL2 are usually of the same size. Crystal manufacturers usually specify the load capacitors as the series combination of CL1 and CL2. When determining CL1 and CL2, PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of combined pin and circuit board capacitance).

Figure 12 Typical Applications of 8MHz Crystals



5.6.1.2 Low-speed external clock

A low-speed external (LSECLK) clock can provide a 32.768kHz crystal resonant oscillator. In the applications, the resonator and load capacitor must be as close as possible to the oscillator pins to minimize output distortion and startup stabilization time.

Table 23 Characteristics OF LSECLK Oscillator (f_{LSECLK}=32.768kHz) (1)

Symbol	Parameter	Condition	Min value	Typ value	Max value	Unit
f_{OSC_IN}	Oscillator frequency	-	-	32.768	-	kHZ
$I_{DD(LSECLK)}$	LSECLK current consumption	-	-	3	-	μA

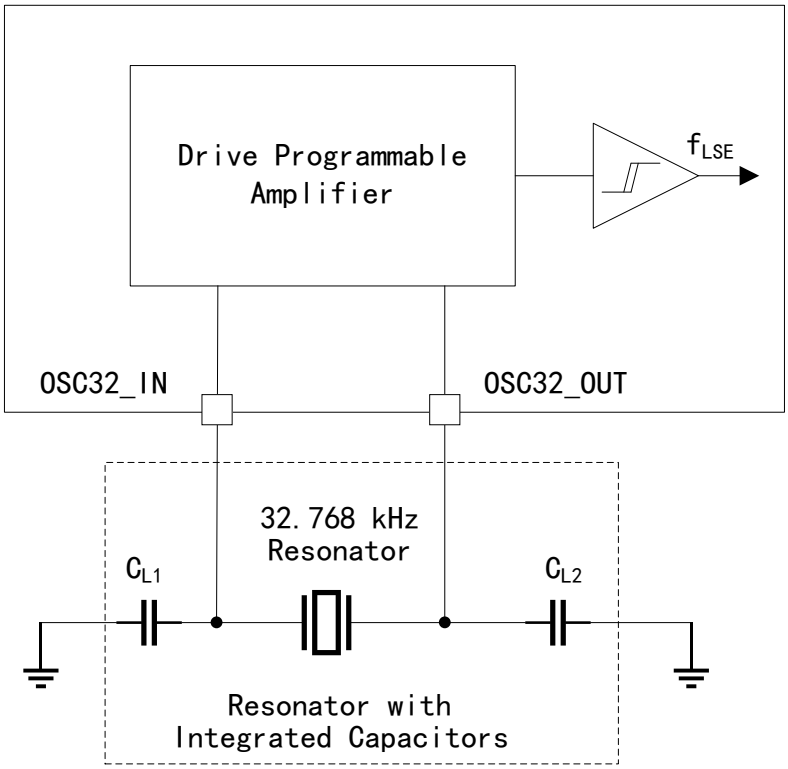
Symbol	Parameter	Condition	Min value	Typ value	Max value	Unit
Gm	Maximum critical crystal transconductance	-	0.5	-	2.70	uA/V
$t_{SU(LSECLK)}$ (2)	Startup time	V_{DD} is stable	-	2	-	s

Note:

(1) The data are obtained from a comprehensive evaluation and are not tested in production.

(2) $t_{SU(LSECLK)}$ is the startup time, which is measured from the software enabling LSECLK until a stable oscillation of 32.768kHz is obtained. This value is measured using a standard crystal resonator, which may vary greatly due to crystal manufacturers.

Figure 13 Typical Applications of 32.768kHz Crystals



5.6.2 Characteristics of internal clock source

5.6.2.1 High-speed internal (HSICLK) RC oscillator

The parameters given in the following table are obtained from tests conducted under general operating ambient temperature and supply voltage. The provided results are characterization results and are not tested in production.

Table 24 Characteristics of HSICLK Oscillator (1)

Symbol	Parameter	Condition	Min value	Typ value	Max value	Unit
f_{HSICLK}	Frequency	-	-	8	-	MHz
TRIM	HSI user trimming step	-	0.05	0.1	0.2	%

Symbol	Parameter	Condition	Min value	Typ value	Max value	Unit
$Duty_{(HSICLK)}$	Duty cycle	-	45	-	55	%
$\Delta_{CC(HSICLK)}$	Accuracy of HSICLK oscillator (calibrated)	V_{DD}=2.7-3.6V，T_A=-40~105℃	-1	-	1	%
		V_{DD}=1.7-3.6V，T_A=-40~105℃	-4	-	4	
$\Delta_{VDD(HSICLK)}$	Frequency drift of HSI oscillator on VDD (calibrated)	V_{DD}=1.7-3.6V,T_A=25℃	-1.5	-	1.5	
$I_{DDA(HSICLK)}$	Power consumption of HSICLK oscillator	-	-	160	200	μA
$t_{STAB(HSICLK)}$	Stabilization time of HSICLK oscillator	-	-	-	5	μs

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.6.2.2 Low-speed internal (LSICLK) RC oscillator

The parameters given in the following table are obtained from tests conducted under general operating ambient temperature and supply voltage. The provided results are characterization results and are not tested in production.

Table 25 Characteristics of LSICLK Oscillator (1)

Symbol	Parameter	Condition	Min value	Typ value	Max value	Unit
f_{LSICLK}	Frequency	V_{DD}=1.7-3.6V, T_A=-40~105℃	29.44	32	34.56	kHZ
$I_{DD(LSICLK)}$	Power consumption of LSICLK oscillator	-	-	0.21	0.27	μA
$t_{STAB(LSICLK)}$	Stabilization time of LSICLK oscillator	5% of final frequency	-	-	300	μs

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.6.3 PLL characteristics

The parameters given in the following table are obtained from tests conducted under general operating ambient temperature and supply voltage. The provided results are characterization results and are not tested in production.

Table 26 PLL Characteristics (1)

Symbol	Parameter	Condition	Min value	Typ value	Max value	Unit
f_{PLL1_IN}	PLL input clock	V_{DD}=1.7-3.6V, T_A=-40~105℃	6	8	26	MHz

Symbol	Parameter	Condition	Min value	Typ value	Max value	Unit
	Duty cycle of PLL input clock	-	45	-	55	%
f_{PLL_OUT}	PLL frequency doubling output clock	V_{DDA}=2.7-3.6V	8	-	128	MHz
		V_{DDA}=1.7-2.7V	8	-	80	
Jitter	Period jitter	System clock 8M~128MHz	8	10	13	ps
t_{LOCK1}	PLL phase locking time	-	10	15	40	μs
$I_{DD(PLL)}$	PLL power consumption	PLL output clock 80MHz	350	410	-	μA
		PLL output clock 128MHz	-	640	-	

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.7 Power Supply and Power Supply Management

5.7.1 Test of embedded reset and power control module characteristics

Table 27 Reset and Power Control Module Characteristics (1)

Symbol	Parameter	Condition	Min value	Typ value	Max value	Unit
$t_{RSTTEMPO}$	Reset duration	The time from detection of POR to execution of the first instruction	-	250	400	μs
$V_{POR/PDR}$(2)	POR/PDR reset threshold	Rising Edge	1.58	1.64	1.68	V
		Falling Edge	1.5	1.56	1.62	
V_{PVD0}	PVD threshold 0	Rising Edge	2.1	2.15	2.19	V
		Falling Edge	2	2.05	2.1	
V_{PVD1}	PVD threshold 1	Rising Edge	2.26	2.30	2.36	V
		Falling Edge	2.15	2.2	2.25	
V_{PVD2}	PVD threshold 2	Rising Edge	2.41	2.45	2.51	V
		Falling Edge	2.31	2.36	2.41	
V_{PVD3}	PVD threshold 3	Rising Edge	2.56	2.60	2.66	V
		Falling Edge	2.47	2.52	2.57	
V_{PVD4}	PVD threshold 4	Rising Edge	2.69	2.75	2.79	V
		Falling Edge	2.59	2.64	2.69	
V_{PVD5}	PVD threshold 5	Rising Edge	2.85	2.90	2.96	V
		Falling Edge	2.75	2.81	2.86	
V_{PVD6}	PVD threshold 6	Rising Edge	2.92	2.98	3.04	V

Symbol	Parameter	Condition	Min value	Typ value	Max value	Unit
		Falling Edge	2.84	2.9	2.96	
$V_{hyst\_POR\_PVD}$	POR/PDR and PVD hysteresis voltage	-	-	80	-	mV

Note:

(1) Guaranteed by design and not tested in production.

(2) The characteristics of the product are guaranteed by design to the minimum value $V_{POR/PDR}$.

5.7.2 Main power detection module (EVS)

Table 28 Characteristics of Main Power Detection Module

Symbol	Parameter	Condition	Min value	Typ value	Max value	Unit
V_{DD}	-	-	3.0	-	3.6	V
V_{PVD0}	Main power detection threshold 0	Rising Edge	4.1	4.3	4.5	V
		Falling Edge	3.96	4.16	4.36	
V_{PVD1}	Main power detection threshold 1	Rising Edge	4.06	4.26	4.46	V
		Falling Edge	3.92	4.12	4.32	
V_{PVD2}	Main power detection threshold 2	Rising Edge	4.15	4.35	4.55	V
		Falling Edge	4	4.2	4.4	
V_{PVD3}	Main power detection threshold 3	Rising Edge	4.2	4.4	4.6	V
		Falling Edge	4.08	4.28	4.48	
V_{hyst}	Hysteresis voltage	-	-	140	-	mV
T_{delay}	Delay time	V_{DDA}=1.7V~3.6V	5	15	40	μs

Note: The rising and falling edge thresholds in VPVDx correspond to the rising and falling edge signals in the EINT module (Stop or Run modes can be configured). When the EVS pin is used for standby wake-up, the wake-up threshold is the threshold corresponding to the rising edge, not the rising or falling edge, which means that as long as the EVS pin level remains above the threshold, it will continuously trigger a wake-up.

5.8 Thermal Resistance Characteristics

Table 29 Thermal Resistance Characteristics of Package

Symbol	Parameter	℃/W (1)			
		UFBGA64	QFN60	QFN48	QFN32
$R\Theta_{JC}$	Thermal resistivity to the shell surface	17.91	11.24	12.25	16.81
$R\Theta_{JB}$	Thermal resistivity to the circuit board	26.46	17.75	17.01	21.1
$R\Theta_{JA}$(high kPCB)	Thermal resistivity to the atmosphere	49.94	35.69	31.25	43.98

Note:

(1) The above values are based on the 2S2P system defined by JEDEC (excluding the values of Theta JC [$R\Theta_{JC}$] of 1S0P system defined based on JEDEC) and will change with the environment and application. For more information, please refer to the following EIA/JEDEC standards:

- JESD51-2, Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)
- JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-9, Test Boards for Area Array Surface Mount Package Thermal Measurements

5.9 Power Consumption

5.9.1 Power consumption test environment

Power consumption testing is conducted under certain conditions:

- The values are measured by executing Coremark, with the KeilV5 compilation environment and the L0 compilation optimization level.
- All I/O pins are in analog input mode and are connected to a static level at V_{DD} or V_{SS} (no load)
- Enable core Cache
- Unless otherwise specified, all peripherals are disabled
- The relationship between Flash wait cycle setting and f_{HCLK}:
  - 0~32MHz: 0 wait cycle
  - 32~64MHz: 1 wait cycles
  - 64~96MHz: 2 wait cycles
  - 96~128MHz: 3 wait cycles
- When the peripherals are enabled: $f_{PCLK}=f_{HCLK}$.

5.9.2 Power consumption in operation mode

Table 30 Power Consumption in Run Mode when the Program is Executed in Flash (1)

Parameter	Condition	f_{HCLK}	Typ value (T_A=25℃)	
			V_{DD}=3.3V	
			I_{DD} (mA)	I_{DDA} (mA)
	HSECLK 8M multiplied clock, PLL enabled, HSICLK disabled, all peripherals enabled (2)	120MHz	21.51	8.42
		96MHz	17.42	8.38
		64MHz	11.70	8.33
		32MHz	6.16	8.28
		16MHz	3.38	8.25
		8MHz	2.48	8.22
	HSECLK 8M multiplied clock, PLL enabled, HSICLK disabled, all peripherals disabled (2)	120MHz	14.63	0.90
		96MHz	11.82	0.86
		64MHz	8.04	0.82
		32MHz	4.24	0.78
		16MHz	2.34	0.77
		8MHz	1.72	0.75

Note:

(1) The data are obtained from a comprehensive evaluation and are not tested in production.

(2) When the analog peripherals such as ADC, HSECLK, LSECLK, HSICLK and LSICLK are turned on, extra power consideration needs to be considered.

5.9.3 Power consumption in stop mode

Table 31 Power Consumption in Stop Mode (1)

Condition		Typ value V_{DD}=3.3V, T_A=25℃
		I_{DD}+I_{DDA} (uA)
Flash is in deep power-down mode, all oscillators are in off state and there is no independent watchdog 32KB ITCM enabled	Voltage regulator (in low-power mode)	7.01
Flash is in deep power-down mode, all oscillators are in off state and there is no independent watchdog 32KB ITCM disabled	Voltage regulator (in low-power mode)	6.80

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

5.9.4 Power consumption in standby mode

Table 32 Power Consumption in Standby Mode (1)

Condition		Typ value V_{DD}=3.3V, T_A=25℃
		$I_{DD}+I_{DDA}$ (uA)
Power supply current in standby mode	LSI and RTC enabled	1.28
	LSI and RTC disabled	1.07

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

5.10 Wake-up Time in Low-power Mode

The measurement of wake-up time in low-power mode is from the start of wake-up event to the time when the user program reads the first instruction, in which V_{DD}=V_{DDA}.

Table 33 Low-power Wake-up Time (T_A=-25℃) (1)

Symbol	Parameter	Condition	Min value	Typ value	Max value	Unit
t_{WUSTOP}	Wake up from stop mode	The regulator is running in low-power mode, and Flash is in deep power-down mode	-	20	-	μs
$t_{WUSTDBY}$	Wake up from standby mode	ADTSLOAD=1 in FLASH_OBSR1	-	50	-	
		ADTSLOAD=0 in FLASH_OBSR1	-	60	-	

Note: (1) The time values in the table are all awakened by an 8MHz HSICLK oscillator as the wake-up clock source. The wake-up time is the time from receiving the wake-up signal to the first instruction after wake-up. The data are obtained from a comprehensive evaluation and are not tested in production.

5.11 I/O port Characteristics

5.11.1 DC characteristics

Unless otherwise specified, the parameters given in the following table are from experiments conducted under ambient temperature and power supply voltage conditions of general operating conditions.

Table 34 DC Characteristics (T_A=-40℃~105℃, V_{DD}=1.7~3.6V) (1)

Symbol	Parameter	Condition	Min value	Typ value	Max value	Unit
V_{IL}	Input low-level voltage	5T, STD and NRST I/O	-	-	0.8	V
V_{IH}	Input high-level voltage	5T, STD and NRST I/O	2	-	-	
V_{hys}	Schmitt trigger hysteresis	5T, STD and NRST I/O	-	350	-	mV
I_{lkg}	Input leakage current	STD I/O, $0 \leqslant V_{IN} \leqslant V_{DD}$	-	-	130	nA

Symbol	Parameter	Condition	Min value	Typ value	Max value	Unit
		5Tf I/O, $0 \leqslant V_{IN} \leqslant V_{DD}$	-	-	10	μA
R_{PU}	Weak pull-up equivalent resistance	$V_{IN}=V_{SS}$	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistance	$V_{IN}=V_{DD}$	30	40	50	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

5.11.2 Characteristics of output drive current

GPIO (General-Purpose Input/Output) can receive or transmit up to ±8mA, and with VOL/VOH relaxed, it can receive or transmit up to ±20mA.

In user applications, the number of I/O pins that can drive current must be limited to ensure that it does not exceed the absolute maximum rated value specified in this manual:

- The sum of the currents of all I/O sources on VDD, and the maximum power consumption of the MCU source on VDD, shall not exceed the absolute maximum rated value ΣI_{VDD}.
- The sum of the currents of all I/O on VSS, and the maximum power consumption of the MCU source on VSS, shall not exceed the absolute maximum rated value ΣI_{VSS}.

5.11.3 AC characteristics

Unless otherwise specified, the parameters given in the following table are from experiments conducted under ambient temperature and power supply voltage conditions of general operating conditions.

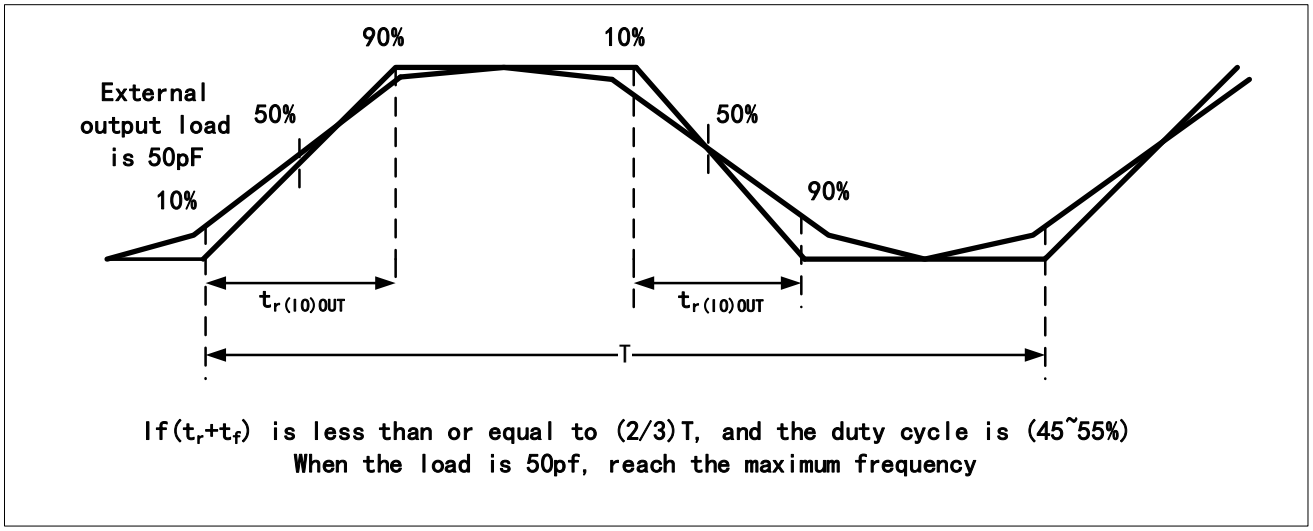
Table 35 AC Characteristics (T_A=25 ℃) (1)

OSPEED[1:0]	Symbol	Parameter	Condition	Min value	Typ value	Max value	Unit
0x	$f_{max(IO)out}$	Maximum frequency	C_L=50pF, $V_{DD} \geqslant 2.0V$	2	-	-	MHz
	$t_{f(IO)out}/t_{r(IO)out}$	Fall time of output from high to low level and rise time of output from low to high level	C_L=50pF, $V_{DD} \geqslant 2.0V$	-	-	125	ns
10	$f_{max(IO)out}$	Maximum frequency	C_L=50pF, $V_{DD} \geqslant 2.0V$	10	-	-	MHz
	$t_{f(IO)out}/t_{r(IO)out}$	Fall time of output from high to low level and rise time of output from low to high level	C_L=50pF, $V_{DD} \geqslant 2.0V$	-	-	25	ns

OSPEED[1:0]	Symbol	Parameter	Condition	Min value	Typ value	Max value	Unit
11	$f_{max(IO)out}$	Maximum frequency	C_L=30pF, $V_{DD}\geqslant$2.7V	50	-	-	MHz
			C_L=50pF, $V_{DD}\geqslant$2.7V	30	-	-	
			C_L=50pF, 2.0V$\leqslant V_{DD}\leqslant$2.7V	20	-	-	
	$t_{f(IO)out}/t_{r(IO)out}$	Fall time of output from high to low level and rise time of output from low to high level	C_L=30pF, $V_{DD}\geqslant$2.7V	-	-	5	ns
			C_L=50pF, $V_{DD}\geqslant$2.7V	-	-	8	
			C_L=50pF, 2.0V$\leqslant V_{DD}\leqslant$2.7V	-	-	12	

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

Figure 14 I/O AC Characteristics Definition



5.11.4 Characteristics of output drive voltage

Unless otherwise specified, the parameters given in the following table are from experiments conducted under ambient temperature and power supply voltage conditions of general operating conditions, and all I/O are CMOS and TTL compatible.

Table 36 Characteristics of Output Drive Voltage (T_A=25 ℃) (1)

Symbol	Parameter	Condition	Min value	Max value	Unit
V_{OL}(2)	I/O pin outputs low voltage	$\|I_{IO}\|$=20mA, 2.7V<V_{DD}<3.6V	-	1.3	V
V_{OH}(2)	I/O pin outputs high voltage		V_{DD}-1.3	-	
V_{OL}(2)	I/O pin outputs low voltage	TTL port, $\|I_{IO}\|$=8mA, 2.7V<V_{DD}<3.6V	-	0.4	
V_{OH}(2)	I/O pin outputs high voltage		V_{DD}-0.4	-	
V_{OL}(2)	I/O pin outputs low voltage	CMOS port, $\|I_{IO}\|$=8mA,	-	0.4	

Symbol	Parameter	Condition	Min value	Max value	Unit
V_{OH}(2)	I/O pin outputs high voltage	2.7V<V_{DD}<3.6V	2.4	-	
V_{OL}(2)	I/O pin outputs low voltage	|I_{IO}|=6mA, 2.0V<V_{DD}<2.7V	-	0.4	
V_{OH}(2)	I/O pin outputs high voltage		V_{DD}-0.4	-	

Note:

(1) The data are obtained from a comprehensive evaluation and are not tested in production.

(2) The I_{IO} current of the I/O input or output must always comply with the absolute maximum rated value specified in this manual.

5.12 NRST Pin Characteristics

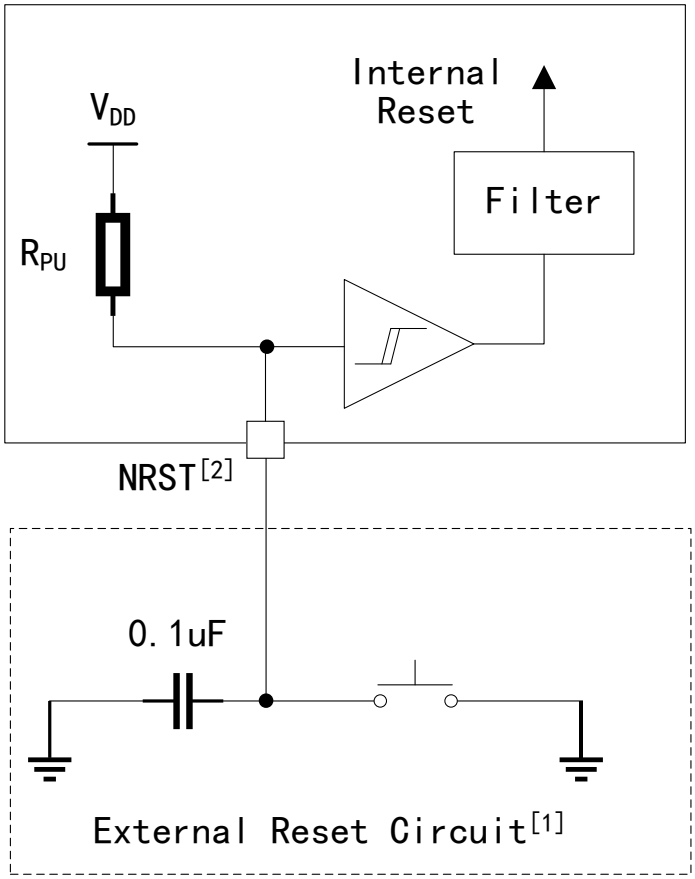
CMOS process is adopted for the NRST pin input drive, which is connected to a permanent pull-up resistor RPU. Unless otherwise specified, the parameters given in the following table are from experiments conducted under ambient temperature and power supply voltage conditions of general operating conditions.

Table 37 NRST Pin Characteristics (T_A=-40~105℃, V_{DD}=1.7V~3.6V) (1)

Symbol	Parameter	Condition	Min value	Typ value	Max value	Unit
V_{IL}	NRST low-level input	-	-	-	0.8	V
V_{IH}	NRST high-level input	-	2	-	-	
V_{hys}	NRST Schmitt trigger voltage hysteresis	-	-	0.3	-	
R_{PU}	Weak pull-up equivalent resistance	V_{IN}=V_{SS}	30	40	50	kΩ
$V_{F(NRST)}$	NRST input filter pulse	-	-	-	100	ns
$V_{NF(NRST)}$	NRST input unfiltered pulse	-	300	-	-	
T_{NRST_OUT}	Generated reset pulse duration	Reset internal source	20	-	-	μs

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

Figure 15 Recommended NRST Pin Protection



5.13 Communication Peripherals

5.13.1 I2C peripheral characteristics

To achieve the maximum frequency of I2C in standard mode, f_{PCLK1} must be greater than 2MHz.

To achieve the maximum frequency of I2C in fast mode, f_{PCLK1} must be greater than 4MHz.

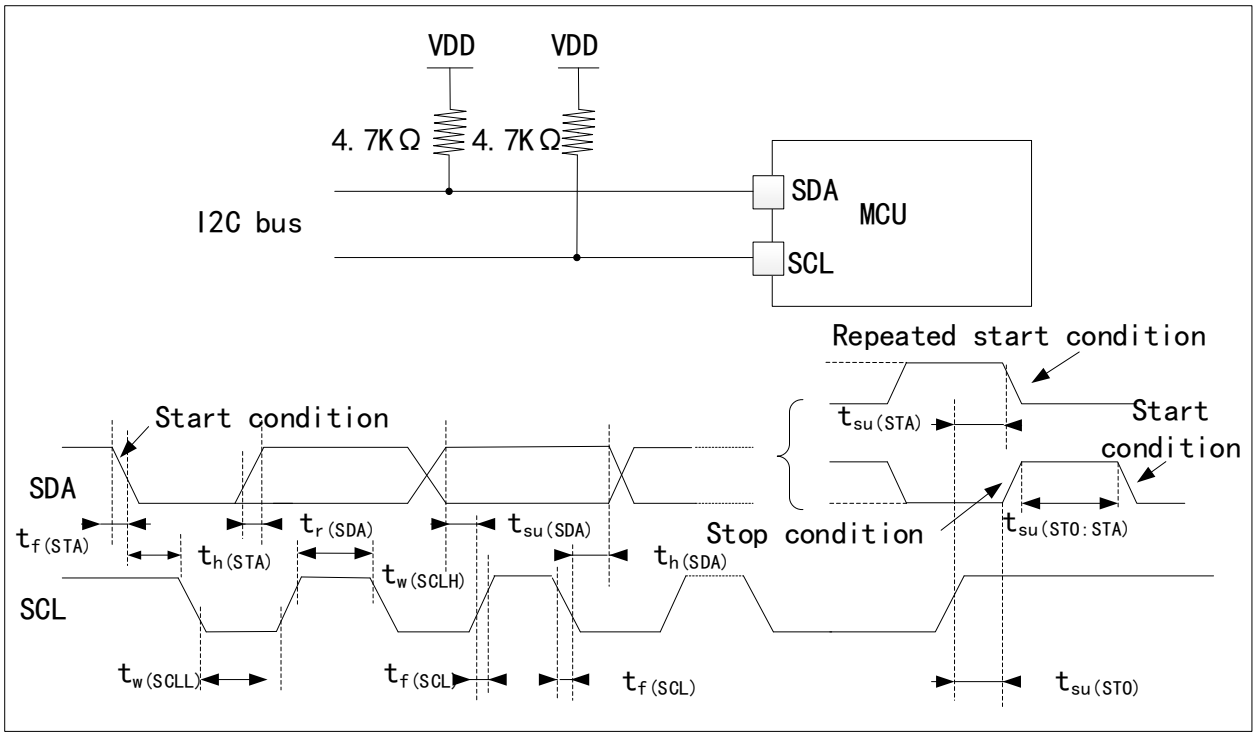
Table 38 I2C Interface Characteristics (T_A=25℃, V_{DD}=3.3V) (1)

Symbol	Parameter	Standard I2C		Fast I2C		Unit
		Min value	Max value	Min value	Max value	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	μs
$t_{w(SCLH)}$	SCL clock high time	4	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0	3450	0	900	
$t_{r(SDA)}/t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}/t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4	-	0.6	-	μs

Symbol	Parameter	Standard I2C		Fast I2C		Unit
		Min value	Max value	Min value	Max value	
$t_{su(STA)}$	Setup time of repeated start condition	4.7	-	0.6	-	
$t_{su(STO)}$	Setup time of stop condition	4	-	0.6	-	
$t_{w(STO:STA)}$	Time from stop condition to start condition (the bus is idle)	4.7	-	1.3	-	
C_b	Capacitive load of each bus	-	400	-	400	pF

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

Figure 16 Bus AC Waveform and Measurement Circuit



Note: The measuring points are set at CMOS levels: 0.3VDD and 0.7VDD.

5.13.2 SPI peripheral characteristics

Table 39 SPI Characteristics (T_A=25℃, V_{DD}=3.3V) (1)

Symbol	Parameter	Condition	Min value	Typ value	Max value	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	-	50	MHz
		Slave mode	-	-	50	
$t_{r(SCK)}$ $t_{f(SCK)}$	SP clock rise and fall time	Load capacitance: C=15pF	-	-	8	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	$4T_{PCLK}$	-	-	
$t_{h(NSS)}$	NSS hold time	Slave mode	$2T_{PCLK}$	-	-	

Symbol	Parameter	Condition	Min value	Typ value	Max value	Unit
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, SPI prescaler=2	T_{PCLK}-1	T_{PCLK}	T_{PCLK}+1	
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	4	-	-	
		Slave mode	3	-	-	
$t_{h(MI)}$ $t_{h(SI)}$	Data input hold time	Master mode	5.5	-	-	
		Slave mode	1	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	9	-	34	
$t_{dis(SO)}$	Disable time of data output	Slave mode	9	-	16	
$t_{v(SO)}$	Effective time of data output	Slave mode (after enabling the edge)	-	9	18	
$t_{v(MO)}$		Master mode (after enabling the edge)	-	3.5	4.5	
$t_{h(SO)}$	Data output hold time	Slave mode (after enabling the edge)	6	-	-	
$t_{h(MO)}$		Master mode (after enabling the edge)	2	-	-	

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

Figure 17 SPI Timing Diagram - Slave Mode and CPHA=0

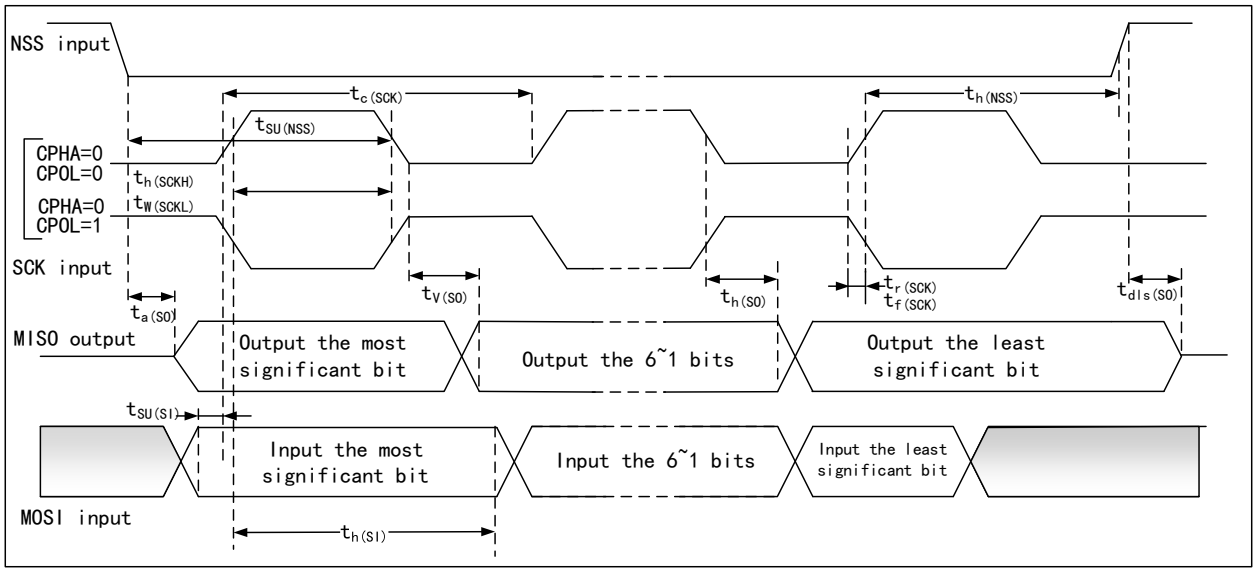
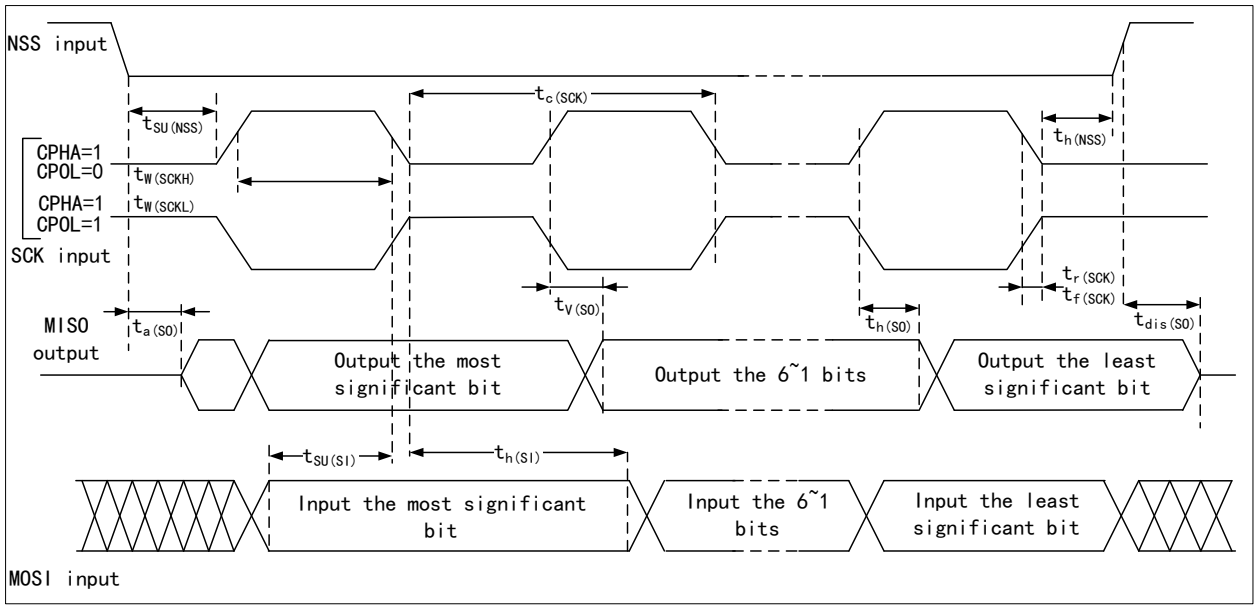
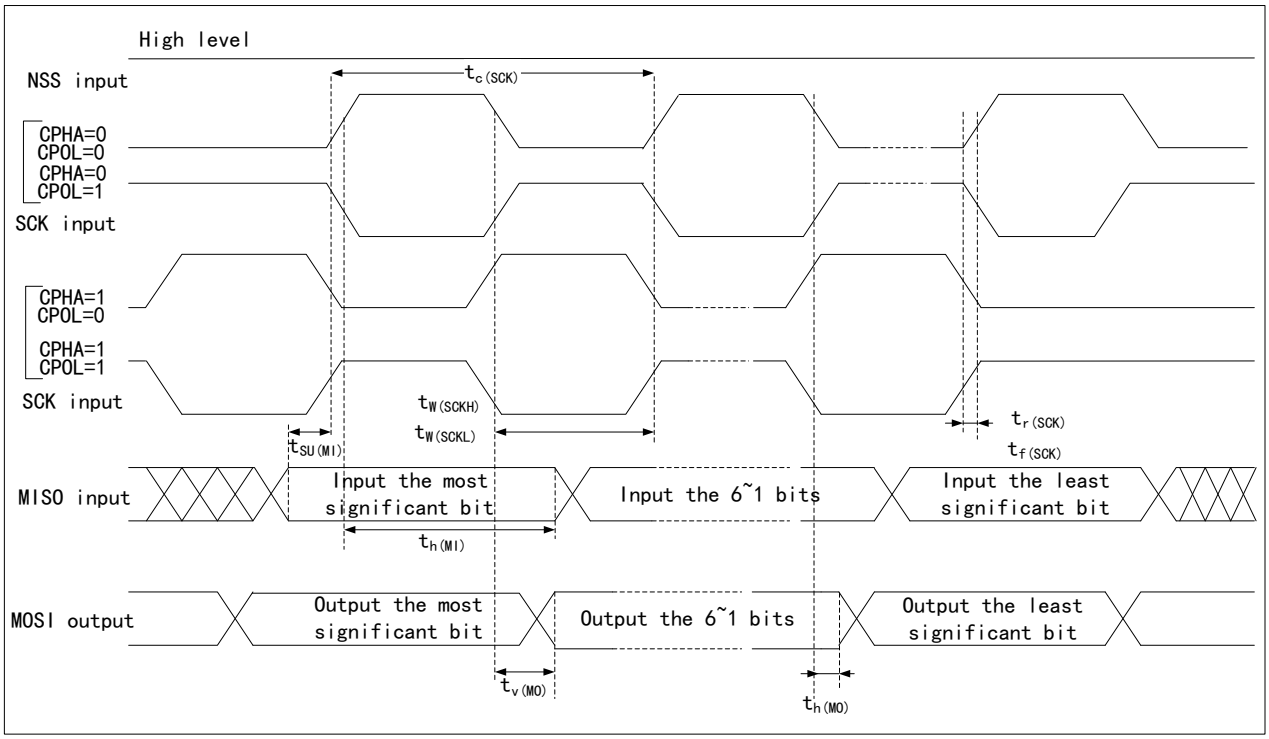


Figure 18 SPI Timing Diagram - Slave Mode and CPHA=1



Note: The measuring points are set at CMOS levels: 0.3VDD and 0.7VDD.

Figure 19 SPI Timing Diagram - Master Mode



Note: The measuring points are set at CMOS levels: 0.3VDD and 0.7VDD.

5.14 ADC Characteristics

ADC test parameter description:

- Sampling rate: The number of conversion of analog quantity to digital quantity by ADC per second

- Sample rate=ADC clock/(the number of sampling periods + the number of conversion cycles)

5.14.1 16-bit ADC characteristics

Table 40 16-bit ADC Characteristics (1) (2)

Conforming	Parameter description	Condition	Min value	Typ value	Max value	Unit
f_{ADC}	ADC clock frequency	f_{HCLK}=128MHz	-	-	f_{HCLK}/6	MHz
V_{DDA}	Analog power supply voltage	-	3.0	-	3.6	V
V_{REF+}	Positive reference voltage	Internal reference voltage mode, T_A=25℃	1.648	1.65	1.652	V
		External reference voltage mode	-	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-	V_{SSA}	-	-	V
$t_{ADCVREG\_STUP}$	ADC regulator startup time	-	-	-	10	ms
t_{STAB}	Power-on time	-	-	10	-	Conversion cycle
V_{AIN} (3)	Conversion voltage range	Internal reference voltage mode	0	-	2*V_{REF+}	V
		External reference voltage mode	0	-	V_{REF+}	V
V_{CMIN}	Input common-mode voltage	Internal reference voltage mode	1.648	1.65	1.652	V
		External reference voltage mode	(V_{REF+}+V_{REF-})/2-0.02	(V_{REF+}+V_{REF-})/2	(V_{REF+}+V_{REF-})/2+0.02	V
f_{sample}	ADC sampling period	In single-ended mode, f_{ADC}=21.3MHz, all ADC are running	5	-	16	1/f_{ADC}
		Differential mode, f_{ADC}=21.3MHz, all ADC are running	3	-	16	1/f_{ADC}
t_S	Sampling time	In single-ended mode, f_{ADC}=21.3MHz, all ADC are running	0.234	-	0.75	μs
		Differential mode, f_{ADC}=21.3MHz, all ADC are running	0.14	-	0.75	μs

Conforming	Parameter description	Condition	Min value	Typ value	Max value	Unit
f_S	Sampling rate, continuous mode, $f_S=f_{ADC}$/(sample time cycles +21)	Single-ended, f_{ADC}=21.3MHz	0.577	-	0.821	Msps
		Differential, f_{ADC}=21.3MHz	0.577	-	0.889	Msps
t_{CONV}	Total conversion time (including sampling time)	Single-ended, f_{ADC}=21.3MHz	1.218	-	1.734	μs
		Differential, f_{ADC}=21.3MHz	1.125	-	1.734	μs
R_{AIN}	External input impedance	-	-	-	1	kΩ
C_{ADC}	Internal sampling and holding capacitance	Internal reference voltage mode	-	3	-	pF
		External reference voltage mode	-	6	-	pF
t_{LATR}	Trigger conversion delay (conventional and injection channels without conversion abort)	$f_{ADC}=f_{HCLK}/6$	2.5	3	3.5	$1/f_{ADC}$
$t_{LATRINJ}$	Trigger conversion delay (termination of injection channel for conventional conversion)	$f_{ADC}=f_{HCLK}/6$	3.5	4	4.5	$1/f_{ADC}$
$I_{DDA(ADC)}$	ADC power consumption (V_{DDA})	$f_S= f_{S(max)}$	-	3000	3300	μA

Note:

(1) Guaranteed by design and not tested in production.

(2) When V_{DDA}<2.4V, enable the I/O analog switch voltage booster (when V_{DDA}<2.4V, enable =1 in SYSCFG_CFGR1). When V_{DDA}≥2.4V, it is disabled.

(3) V_{REF}+ can be internally connected to the VDDA pin, depending on the package option.

Table 41 16-bit ADC Accuracy (T_A=-40℃~105℃)

Symbol	Parameter description	Test condition	Mode	Typ value	Max value	Unit
E_O	Offset error	f_{HCLK}=128MHz, $f_{ADC}=f_{HCLK}/6$,	Single-ended mode	±5	-	LSB
			Differential mode		-	

Symbol	Parameter description	Test condition	Mode	Typ value	Max value	Unit
E_G	Gain error	External reference voltage (After calibration)	Single-ended mode	±5	-	
			Differential mode		-	
E_T	Composite error		Single-ended mode	±10	-	
			Differential mode		-	
E_D	Differential linear error	f_{HCLK}=128MHz, f_{ADC}= f_{HCLK}/6	Single-ended mode	±2.5	-	
			Differential mode	±3	-	
E_L	Integral linear error		Single-ended mode	±10	-	
			Differential mode	±10	-	
ENOB	Effective number of bits	f_{HCLK}=128MHz, f_{ADC}=f_{HCLK}/6, V_{REF}+=1.65V (internal reference voltage), Input signal frequency=100kHz	Single-ended mode	12.1	-	bits
			Differential mode	13.3	-	
SINAD	Signal-to-noise ratio and distortion ratio		Single-ended mode	74.6	-	dB
			Differential mode	81.1	-	
SNR	Signal-to-noise ratio		Single-ended mode	74.5	-	
			Differential mode	82.3	-	
THD	Total harmonic distortion		Single-ended mode	-88.1	-	
			Differential mode	-94.4	-	
ENOB	Effective Number of Bits	f_{HCLK}=128MHz f_{ADC}=f_{HCLK}/6, V_{REF}+=V_{DDA} (external reference voltage) Input signal frequency=100kHz	Single-ended mode	12.5	-	bits
			Differential mode	13.6	-	
SINAD	Signal-to-noise ratio and distortion ratio		Single-ended mode	77.0	-	dB
			Differential mode	83.6	-	

Symbol	Parameter description	Test condition	Mode	Typ value	Max value	Unit
SNR	Signal-to-noise ratio		Single-ended mode	77.7	-	
			Differential mode	84.7	-	
THD	Total harmonic distortion		Single-ended mode	-86.5	-	
			Differential mode	-91.2	-	

Note: Guaranteed by design and not tested in production.

5.14.2 12-bit ADC characteristics

Table 42 12-bit ADC Characteristics

Symbol	Parameter description	Condition	Min value	Typ value	Max value	Unit
f_{ADC}	ADC clock frequency	-	-	-	20	MHz
V_{DDA}	Supply voltage	-	2.7	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.7	-	V_{DDA}	V
t_S	Sampling time	f_{ADC}=20MHz	0.35	-	12.8	μs
			7	-	256	$1/f_{ADC}$
f_S	Sampling rate $f_S=f_{ADC}/$(sample time cycles +13)	f_{ADC}=20MHz	0.074	-	1	MHz
V_{AIN}	Conversion voltage range	-	0	-	V_{REF+}	V
R_{ADC}	Sampling resistor	-	-	-	1	kΩ
C_{ADC}	Sampling and holding capacitance	-	-	6	-	pF

Note: Guaranteed by design and not tested in production.

Table 43 12-bit ADC Accuracy (1)

Symbol	Parameter description	Condition	Typ value	Max value	Unit
E_T	Composite error	f_{ADC}=20MHz, V_{DDA}=2.7V~3.6V	± 2.5	-	LSB
E_O	Offset error		± 1.0	-	

Symbol	Parameter description	Condition	Typ value	Max value	Unit
E_G	Gain error	T_A=-40℃~105℃ Input signal frequency=27.5kHz	±1.0	-	
E_D	Differential linear error		±1.0	-	
E_L	Integral linear error		±3.5	-	
ENOB	Effective number of bits		10.1	-	bits
SINAD	Signal-to-noise ratio and distortion ratio		62.6	-	dB
SNR	Signal-to-noise ratio		69.9	-	
THD	Total harmonic distortion		-63.9	-	

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

5.15 Temperature Sensor Characteristics

Table 44 Characteristics of Temperature Sensor

Symbol	Parameter description	Condition	Min value	Typ value	Max value	Unit
V_{DDA}	Analog power supply voltage	-	2.7	3.3	3.6	V
T_{INL}	INL (calibrated)	T_A=-40~105℃	-	-	1.28	°C
T_G	Gain error (calibrated)		-	2.5	-	
T_O	Offset error (calibrated)		-	-	0.7	
$I_{DD(TS)}$	Current consumption of temperature sensor		-	550	-	μA
$t_{startup}$	Time from power-on to the stabilization of module sampling		-	10	-	ms

Note: Guaranteed by design and not tested in production.

5.16 LTCBG Reference Voltage

Table 45 LTCBG Characteristics

Symbol	Parameter description	Condition	Min value	Typ value	Max value	Unit
V_{DDA}	-	-	1.7	3.3	3.6	V
$VREF_{LTCBG}$	Output voltage	-	-	1.08	-	V
$\Delta VREF_{LTCBG\_TC}$	Temperature characteristics of output voltage	Tj= -40~125 °C	-	23	-	ppm
$\Delta VREF_{LTCBG\_VC}$	Voltage characteristics of output voltage	V_{DDA}=1.7V~3.6V	-	44	-	ppm
I_{LTCBG}	Current	-	-	85	-	uA

Symbol	Parameter description	Condition	Min value	Typ value	Max value	Unit
T_{STABLE}	Stability time	-	-	-	45	μs

5.17 Comparator Characteristics

Table 46 Characteristics of COMP

Symbol	Parameter	Condition	Min value	Typ value	Max value	Unit
V_{DDA}	-	-	2.7	3.3	3.6	V
G_{OL}	Open-loop gain	-	-	82	-	dB
V_{min}	Comparator resolution	-	300	-	-	uV
V_O	Input offset voltage	2.7V<V_{IN}<3.6V, -40℃<T_A<105℃	-18	-	18	mV
V_{hys}	Hysteresis voltage	HYS[1:0]=0b00	-	0	-	mV
		HYS[1:0]=0b01	-	24	-	
		HYS[1:0]=0b10	-	45	-	
		HYS[1:0]=0b11	-	65	-	
T_d	Response time	Step response	-	50	-	ns
		The time from comparator enable signal to output change	-	130	-	
I_{comp}	Consumption current	-	-	126	-	uA

5.18 DAC Characteristics

Table 47 DAC Characteristics (1)

Symbol	Parameter description	Condition	Min value	Typ value	Max value	Unit
V_{DDA}	Analog power supply voltage	-	2.7	-	3.6	V
V_{DAC_REF+}	Positive reference voltage	-	-	-	V_{DDA}	
V_{DAC_REF-}	Negative reference voltage	-	V_{SSA}	-	-	
V_{DAC_OUT}	Output voltage	-	0.3	-	V_{DDA}-0.3	
C_L	Load capacitance	Internal channel	-	-	1	pF

Symbol	Parameter description	Condition	Min value	Typ value	Max value	Unit
		External channel	-	-	50	
$t_{SETTLING}$	Setup time	Internal channel	-	-	600	ns
		External channel	-	-	1000	
$I_{DDA(DAC)}$	Current consumed from V_{DDA}	-	-	480	632	uA

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

Table 48 DAC Accuracy (Based on 1MSPS Accuracy)

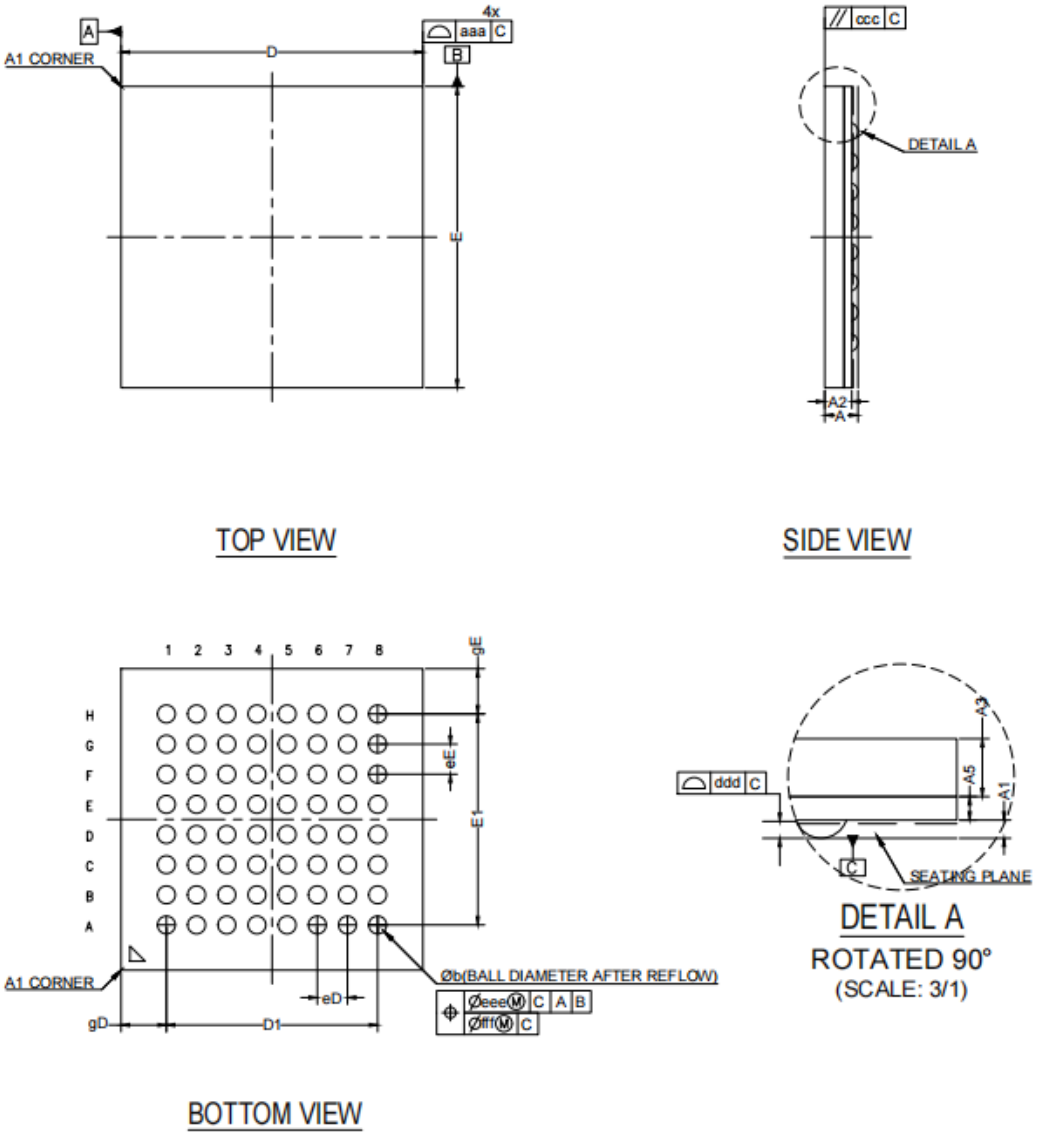
Symbol	Parameter	Condition	Min value	Typ value	Max value	Unit
E_O	Offset error	-	-	-	±10	mV
E_G	Gain error	-	-	-	±0.5	%
E_T	Composite error	-	-	-	±5	LSB
E_D	Differential nonlinearity	-	-	-	±1	
E_L	Integral nonlinearity	-	-	-	±2	
ENOB	Effective number of bits	-	-	9.4	-	bits
SNR	Signal-to-noise ratio	-	-	58.4	-	dB
SINAD	Signal-to-noise ratio and distortion ratio	-	-	58.2	-	
THD	Total harmonic distortion	-	-	-69.7	-	

Note: The data are obtained from a comprehensive evaluation and are not tested in production.

6 Package Information

6.1 UFBGA64 Package Information

Figure 20 UFBGA64 Package Diagram



Note: The figure is not drawn to scale.

Table 49 UFBGA64 Package Data

ITEM		SYMBOL	COMMON DIMENSIONS		
			MIN.	NOM.	MAX.
Body Size	X	D	4.900	5.000	5.100
	Y	E	4.900	5.000	5.100

ITEM		SYMBOL	COMMON DIMENSIONS		
			MIN.	NOM.	MAX.
Ball Pitch	X	eD	0.500		
	Y	eE	0.500		
Total Thickness		A	0.460	0.550	0.620
Ball Stand Off		A1	0.070	0.100	0.130
Mold+Substrate		A2	0.400	0.450	0.500
Mold Thickness		A3	0.280	0.320	0.360
Substrate Thickness		A5	0.100	0.130	0.160
Raw Ball Size		b'	0.210		
Ball Size (After Reflow)		b	0.245	0.295	0.345
Package Edge Tolerance		aaa	0.150		
Mold Flatness		ccc	0.200		
Coplanarity		ddd	0.080		
Ball Offset (Package)		eee	0.150		
Ball Offset (Ball)		fff	0.050		
Ball Count		n	64		
Edge Ball Center to Center	X	D1	3.500		
	Y	E1	3.500		
Edge Ball Center to Package Edge	X	gD	0.750		
	Y	gE	0.750		

Note:

(1) Dimensions are marked in millimeters.

(2) All dimensions and tolerances comply with ASME Y14.5M-2009 standard.

(3) Pin positions are marked based on JESD 95 standard.

(4) The dimension "b" is measured at the maximum solder ball diameter, parallel to the main reference C.

(5) The opening diameter of the solder mask on BGA pads is Ø0.29 millimeter.

Figure 21 UFBGA64 Welding Layout Recommendations

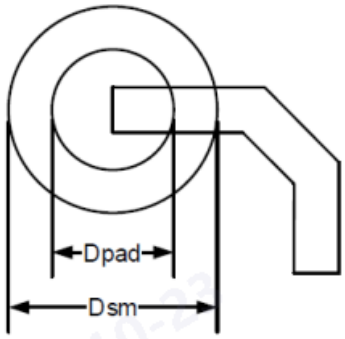
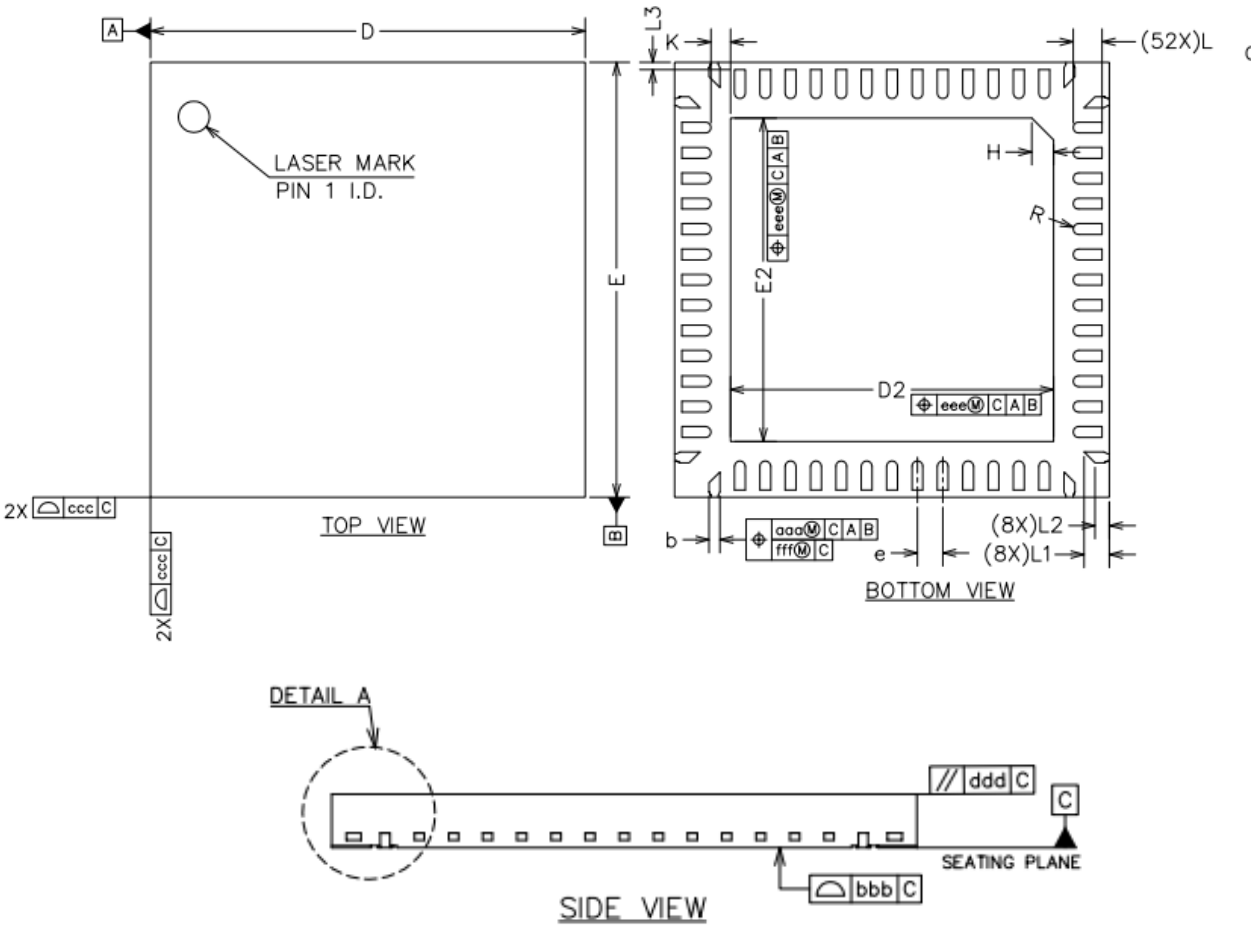


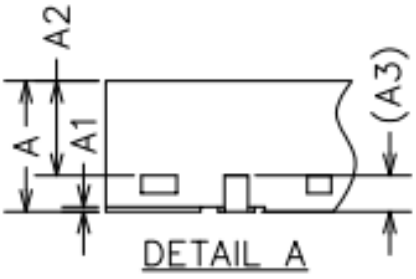
Table 50 Instructions of Layout Recommendations for UFBGA64 Welding

Dimension	Recommended values
Pitch	0.5 mm
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm

6.2 QFN60 Package Information

Figure 22 QFN60 Package Diagram





Note:

(1) The figure is not drawn to scale.

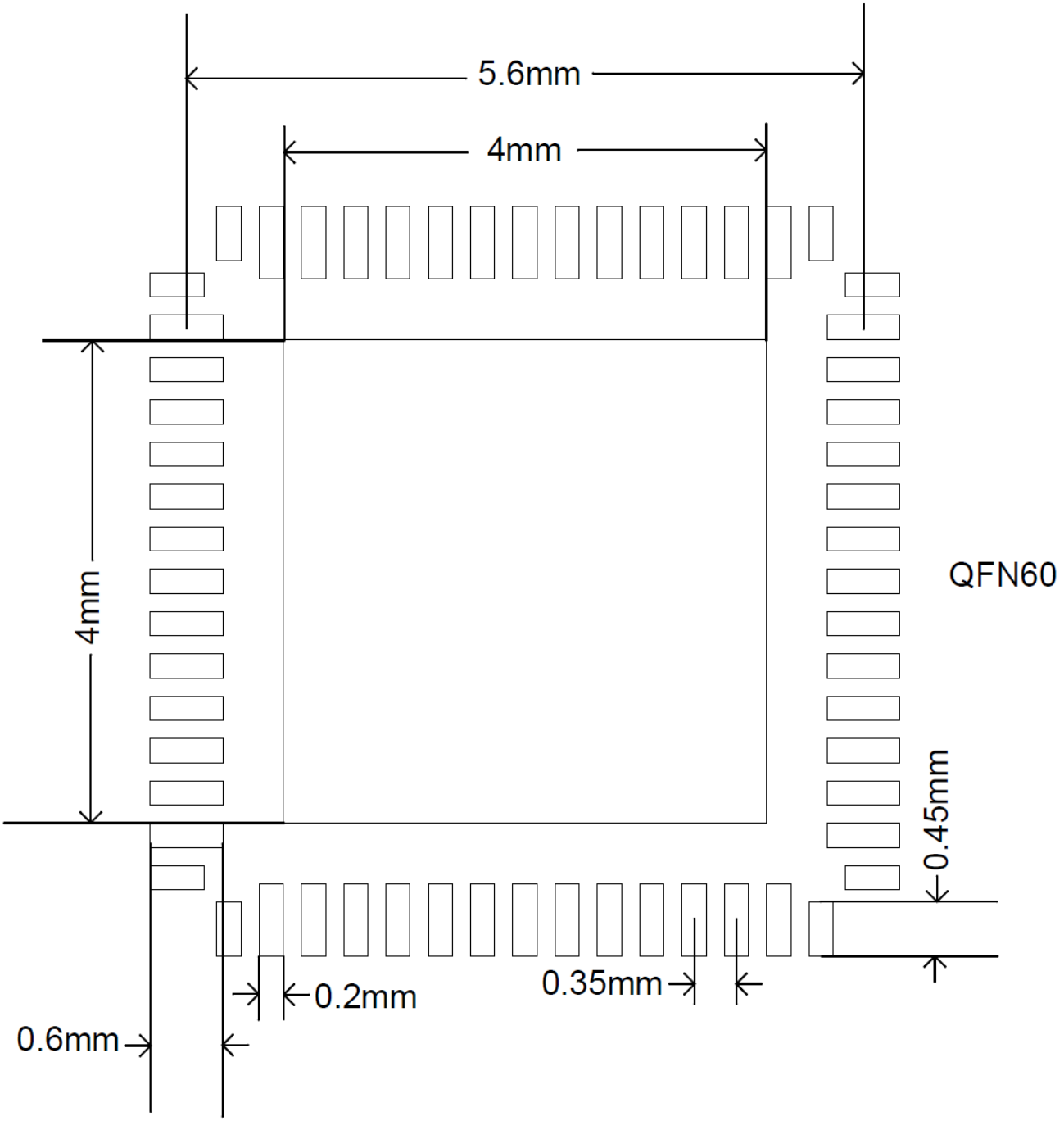
(2) All pins should be soldered to the PCB.

Table 51 QFN60 Package Data

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A2	0.35	0.40	0.45
A3	0.152REF		
b	0.10	0.15	0.20
D	5.90	6.00	6.10
E	5.90	6.00	6.10
D2	4.36	4.46	4.56
E2	4.36	4.46	4.56
e	0.35BSC		
H	0.30REF		
K	0.17	0.27	0.37
L	0.35	0.40	0.45
L1	0.299	0.349	0.399
L2	0.149	0.199	0.249
L3	0.05	0.10	0.15
R	0.05	-	-
aaa	0.07		
bbb	0.08		
ccc	0.10		
ddd	0.10		
eee	0.10		

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
fff		0.05	

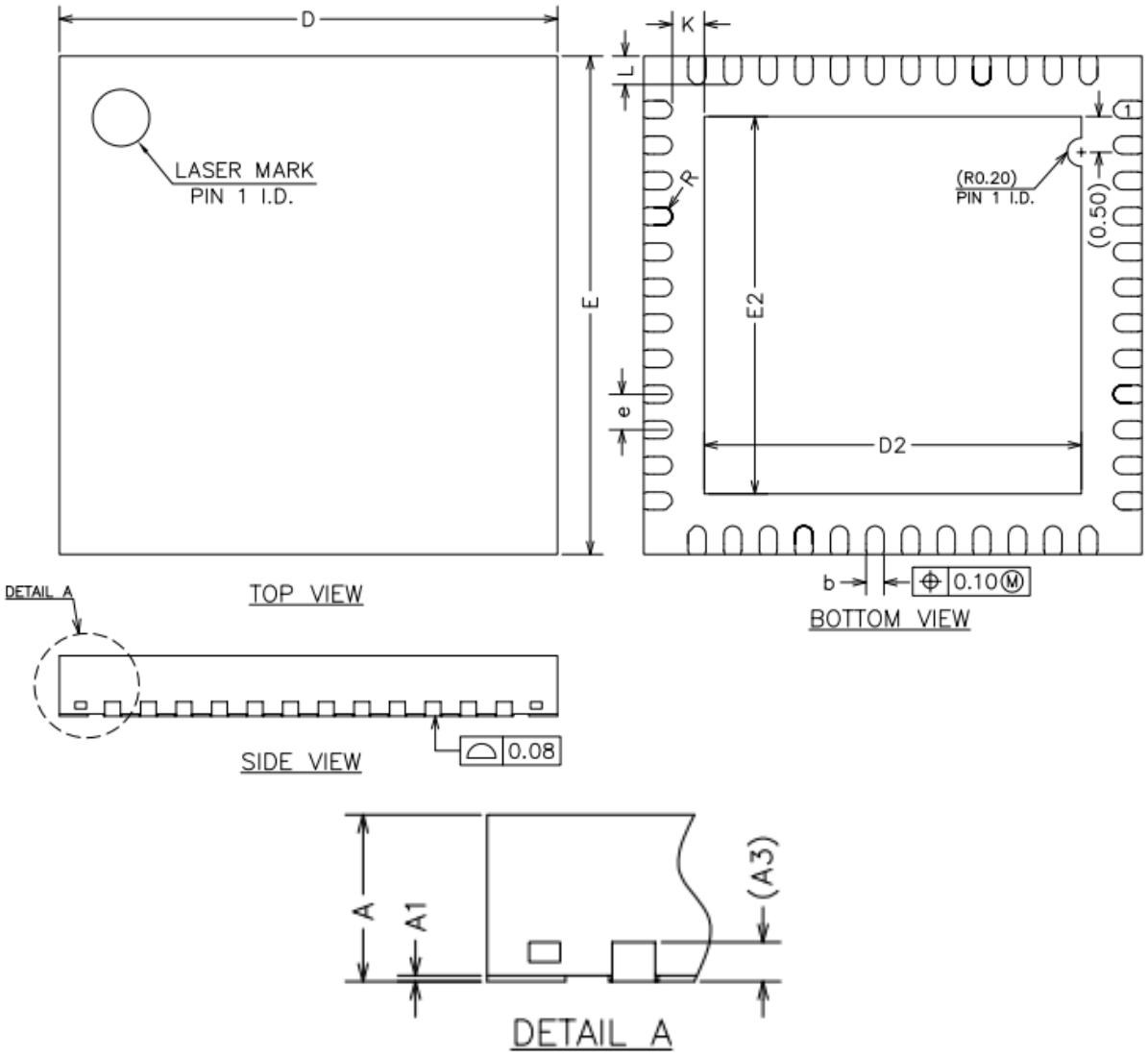
Figure 23 QFN60 Welding Layout Recommendations



Note: Dimensions are marked in millimeters.

6.3 QFN48 Package Information

Figure 24 QFN48 Package Diagram



Note:

(1) The figure is not drawn to scale.

(2) All pins should be soldered to the PCB.

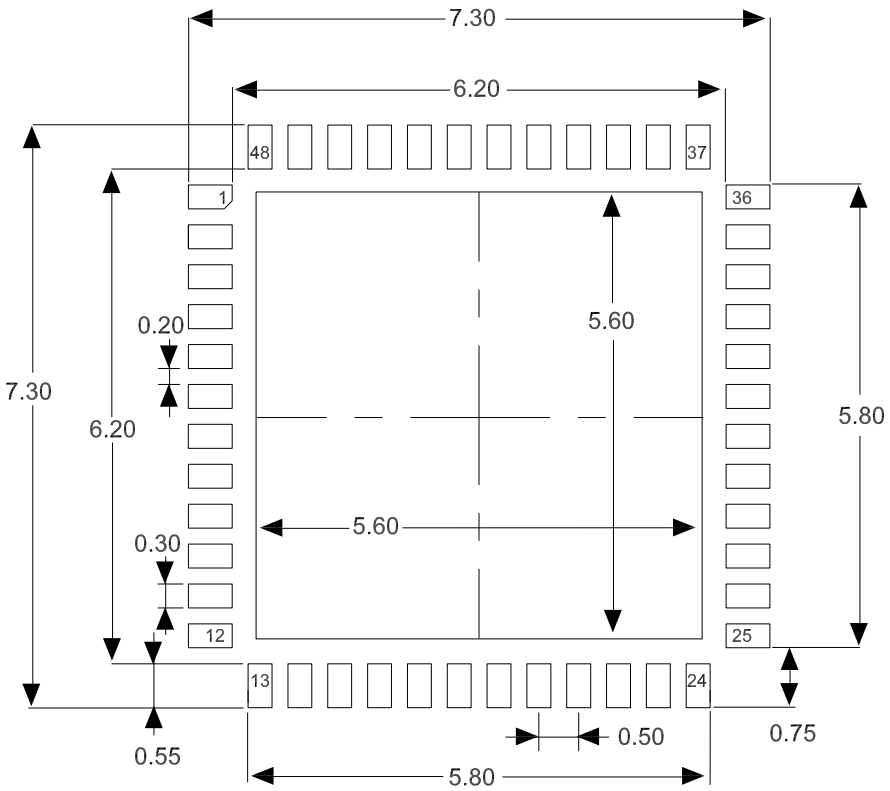
Table 52 QFN48 Package Data

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20REF		
b	0.20	0.25	0.30

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D2	5.20	5.30	5.40
E2	5.20	5.30	5.40
e	0.40	0.50	0.60
K	0.35	0.45	0.55
L	0.30	0.40	0.50
R	0.09	-	-

Note: Dimensions are marked in millimeters.

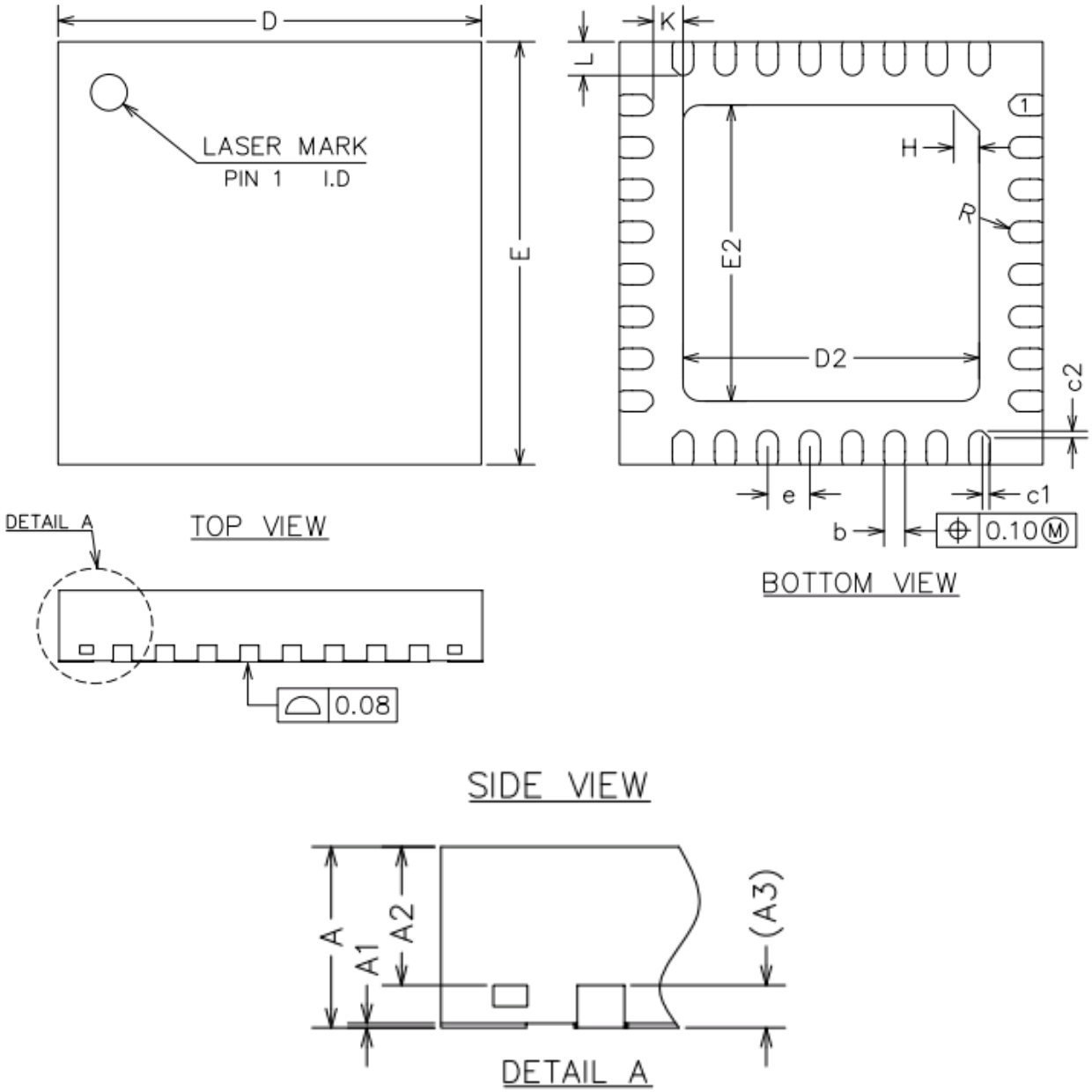
Figure 25 QFN48 Welding Layout Recommendations



Note: Dimensions are marked in millimeters.

6.4 QFN32 Package Information

Figure 26 QFN32 Package Diagram



Note:

(1) The figure is not drawn to scale.

(2) All pins should be soldered to the PCB.

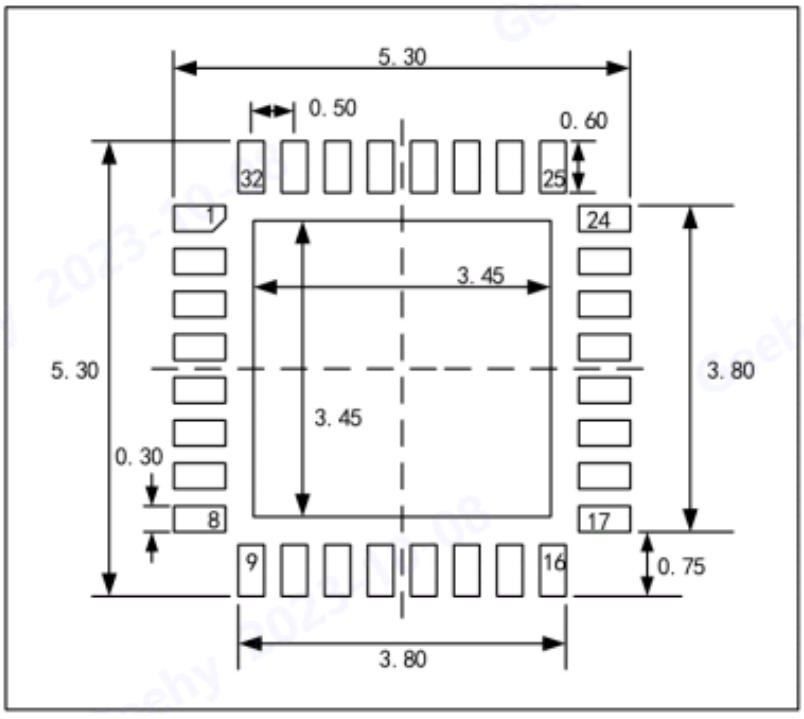
Table 53 QFN32 Package Data

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A2	0.50	0.55	0.60
A3	0.20REF		
b	0.20	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.40	3.50	3.60
E2	3.40	3.50	3.60
e	0.40	0.50	0.60
H	0.30REF		
K	0.35REF		
L	0.35	0.40	0.45
R	0.09	-	-
c1	-	0.08	-
c2	-	0.08	-

Note: Dimensions are marked in millimeters.

Figure 27 QFN32 Welding Layout Recommendations



6.5 Package Identification

Figure 28 UFBGA and QFN Package Designator

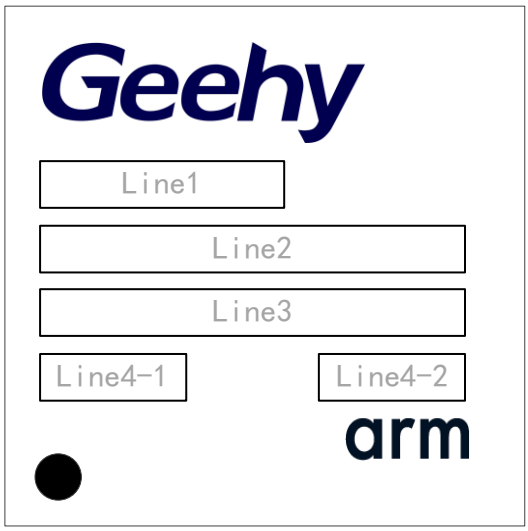


Table 54 UFBGA and QFN silk-screen printing figure description

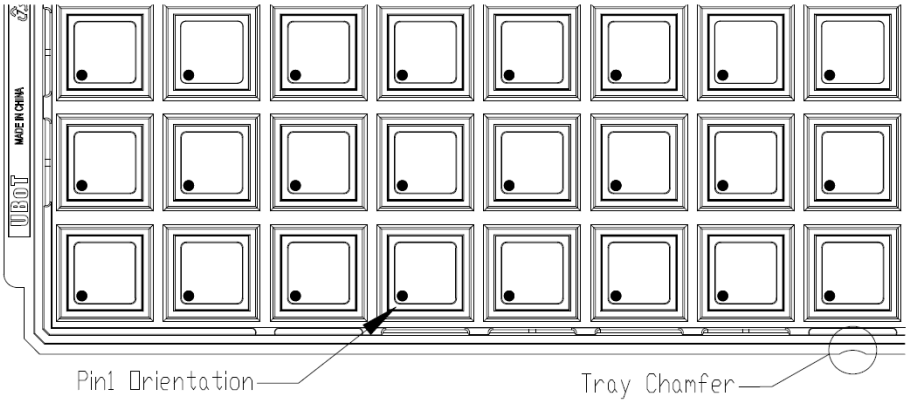
Symbols and Icons	description
Geehy	Geehy
Line1	Product Series
Line2	product model
Line3	batch number
Line4-1	Internal traceability code
Line4-2	Year and week number
arm	Arm® authorization identification
●	PIN1 location

Note: The number of digits in each column above is not fixed.

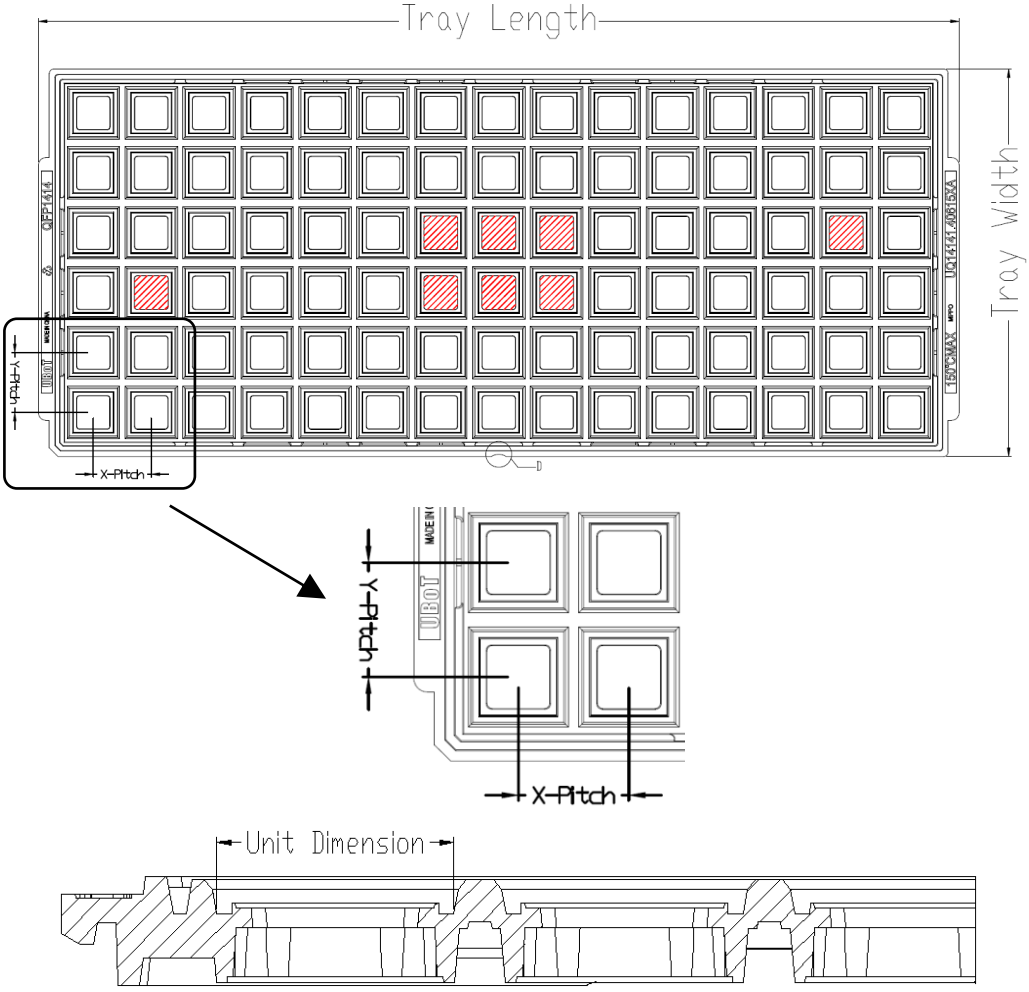
7 Packaging Information

7.1 Tray Packaging

Figure 29 Tray Packaging Diagram



Tray Dimensions



Note: All photos are for reference only, and the appearance is subject to the product.

Table 55 Parameter Specification Table of Tray Packaging

Device	Package Type	Pins	SPQ	X-Dimension (mm)	Y-Dimension (mm)	X-Pitch (mm)	Y-Pitch (mm)	Tray Length (mm)	Tray Width (mm)
G32R430RBI7	UFBGA	64	4900	5.2	5.2	8.8	9.2	322.6	135.9
G32R430UBU7	QFN	60	4900	6.2	6.2	8.8	9.2	322.6	135.9
G32R430CBU7	QFN	48	2600	7.25	7.25	11.8	12.8	322.6	135.9
G32R430KBU7	QFN	32	4900	5.2	5.2	8.7	9.0	322.6	135.9

8 Ordering Information

Table 56 Product Naming Definition

Product name			
G32R430RBI7			
Naming example	**Definition**	**Naming**	**Information**
G32	Product series	G32	32-bit microcontroller based on Arm
R	Product type	R	Real-time control
430	Product subseries	430	Encoder application
R	Number of pins	K	32 pins
		C	48 pins
		U	60 pins
		R	64 pins
B	Flash memory capacity	B	128KB
I	Package	U	QFN
		I	UFBGA (Pitch 0.5)
7	Temperature range	7	Industrial-grade temperature range: -40℃~105℃
Blank	Option	XXX	Programmed device code
		Blank	Tray packaging
		R	Reel packaging
		T	Tube packaging

Table 57 Ordering Information List

Order code	FLASH(KB)	DTCM(KB)	ITCM(KB)	SPQ	Package	Packaging	Temperature range
G32R430RBI7	128	16	32	4900	UFBGA64	Tray	-40℃ ~ 105℃
G32R430UBU7	128	16	32	4900	QFN60	Tray	-40℃ ~ 105℃
G32R430CBU7	128	16	32	2600	QFN48	Tray	-40℃ ~ 105℃
G32R430KBU7	128	16	32	4900	QFN32	Tray	-40℃ ~ 105℃

Note: SPQ means Smallest Packaging Quantity

9 Denomination of Commonly Used Function Module

Table 58 Denomination of Commonly Used Function Modules

Full name	Abbreviation
Reset Management Unit	RMU
Clock management unit	CMU
Reset and clock management	RCM
Trigonometric mathematical unit	TMU
Adaptive real-time memory accelerator	ART
Nested Vector Interrupt Controller	NVIC
External Interrupt	EINT
General-purpose IO	GPIO
Multiplexing IO	AFIO
Wake-up controller	WUC
Independent watchdog timer	IWDT
Window watchdog timer	WWDT
Timer	TMR
Low-power timer	LPTMR
Power management unit	PMU
DMA controller	DMA
Analog-to-digital converter	ADC
Temperature sensor	TSEN
Digital-to-analog converter	DAC
Comparator	COMP
Real-time Clock	RTC
Backup domain	BKP
I2C Interface	I2C
Serial Peripheral Interface	SPI
Universal synchronous and asynchronous receiver transmitter	USART

10 Revision History

Table 59 Document Revision History

Date	Version	Revision History
December 2025	0.1	• Initial version
January 2026	0.2	• Modified the FLASH and power consumption data
February 2026	0.3	• Modified the function of COMP in the "Pin Function Description" section • Modified the note in "4.3.1"

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8. Scope of application

The information in this manual replaces the information provided in all previous versions of the manual.